Analog IC Design Automation

Tools and Methods to Assist Analog IC Designers

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INSTITUIÇÕES ASSOCIADAS:

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creating and sharing knowledge for telecommunications

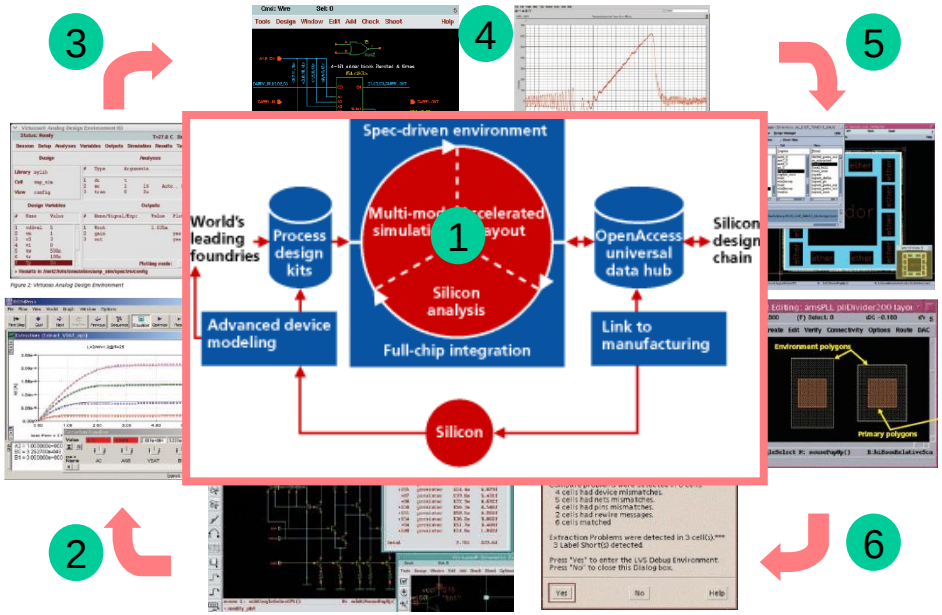
OUTLINE

- Motivation
- Analog IC DA: Overview
- ICG DA Tools and Methods:
  - Circuit-Level Synthesis: GENOM-POF (N. Lourenço, N. Horta)
  - Layout-Level Synthesis: LAYGEN II (R. Martins, N. Lourenço, N. Horta)
- Conclusions

MOTIVATION

ANALOG IC Design and CAD tools

- Are available to handle typical design flows
- Cadence and HSPICE are Schematic and simulation oriented
- Designers need to apply their expertise for simulation and resizing which is largely crafted by hand
- Assisted simulation and resizing is considered the most time consuming process
- Lack of commercial DA tools at both circuit and layout–level synthesis.



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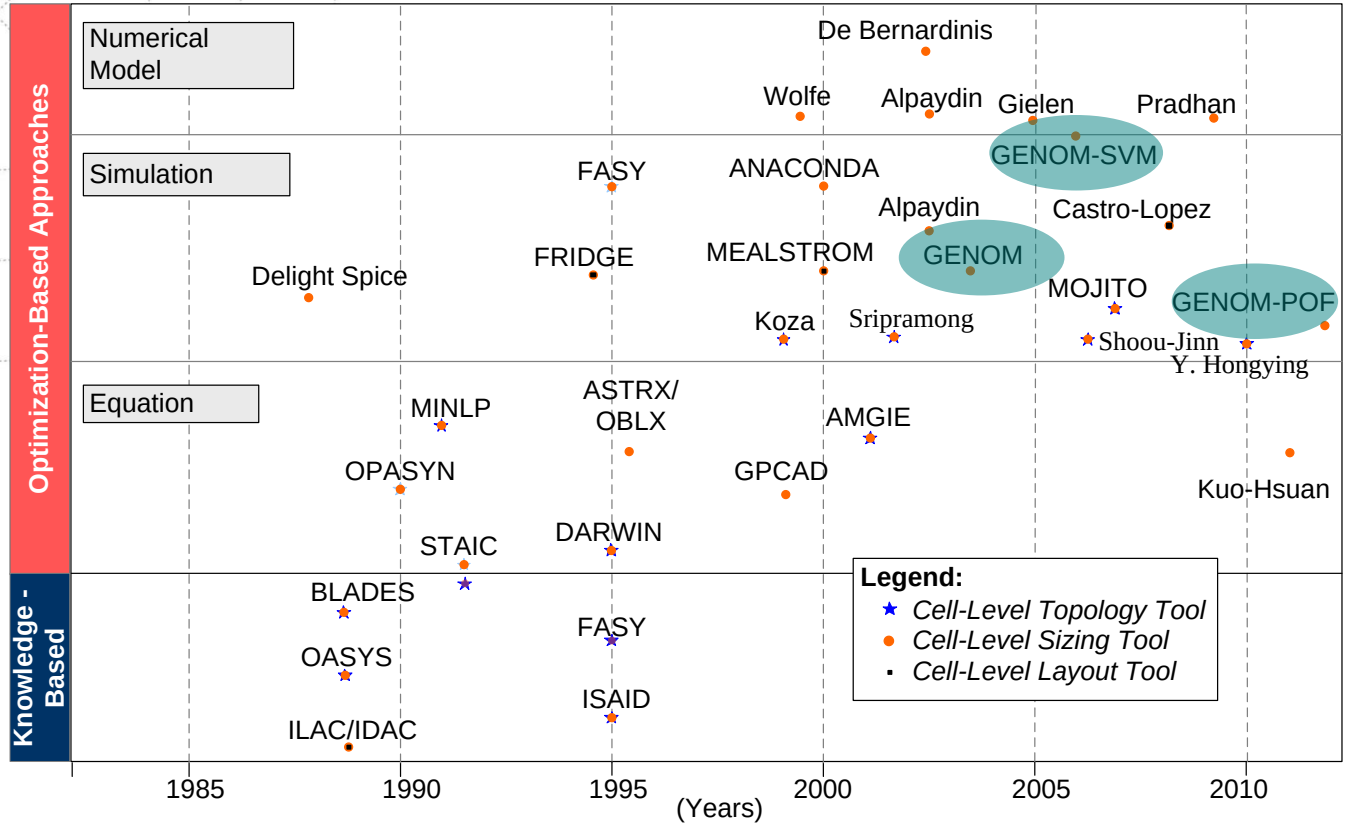
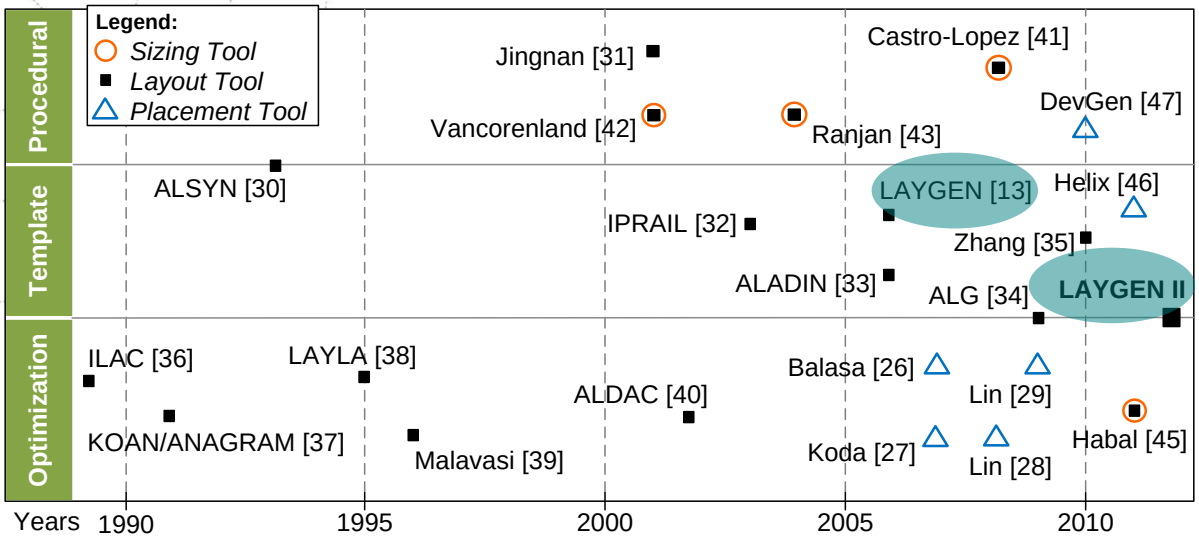
ANALOG IC DA: OVERVIEW (CIRCUIT-LEVEL SYNTHESIS)

Tools and Methods Evolution



ANALOG IC DA: OVERVIEW (LAYOUT-LEVEL SYNTHESIS)

Tools and Methods Evolution



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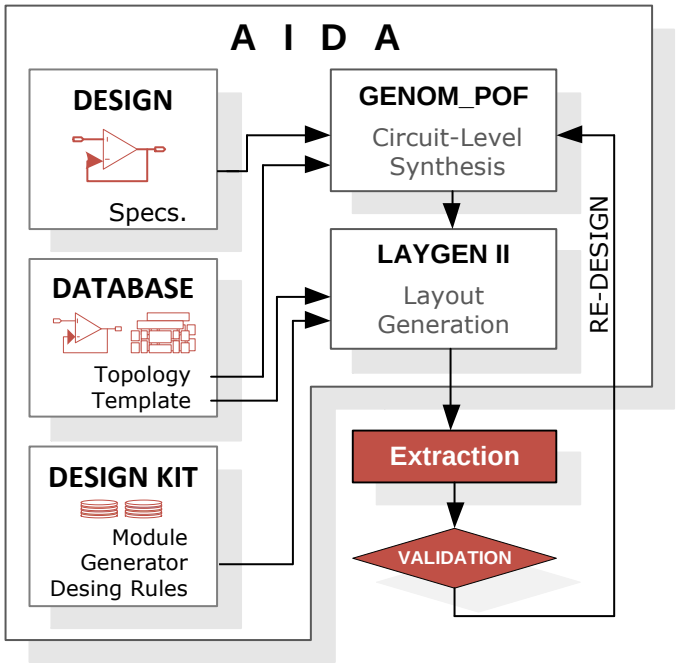
CASE STUDIES

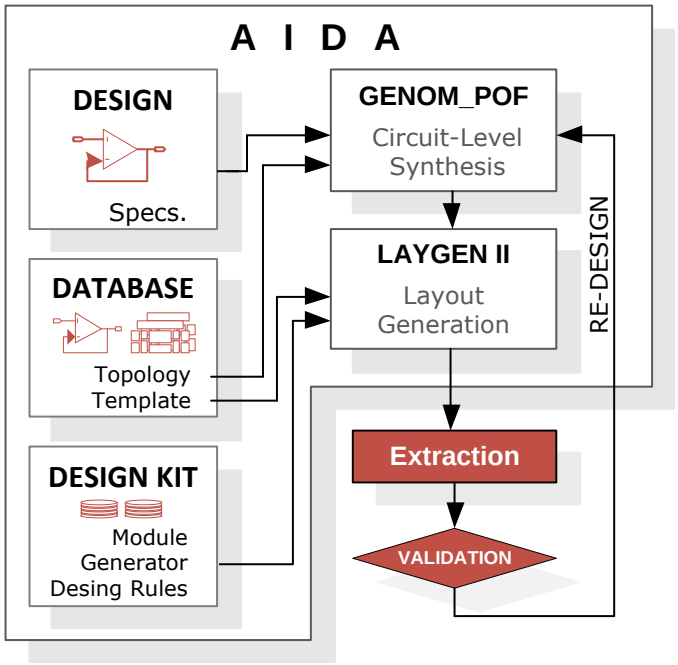
AIDA – Analog IC Design Automation Environment (1 of 3)



- **AIDA** results from the integration of GENOM-POF and LAYGEN-II
- **GENOM-POF**: Circuit-Level Synthesis
  - Multi-objective Multi-constraint Optimization-based Approach
  - Robust design: Corners validation and Electrical Simulation
- **LAYGEN II**: Layout-Level Generation
  - Template-based Approach
  - DRC proved fully automated layout generation

CASE STUDIES

AIDA – Analog IC Design Automation Environment (2 of 3)



- **LEVEL of AUTOMATION**
  - from circuit to layout
- **DOMAIN and PROBLEM COMPLEXITY**
  - circuit synthesis and layout generation
  - optimization problem complexity (CL) – modified NSGA-II Kernel
  - circuit complexity (CL) – SVM models to prune search space
  - optimization problem complexity (LL) – Hierarchical Template Descrip.
  - circuit complexity (LL) – built-in DRC evaluation engine

CASE STUDIES

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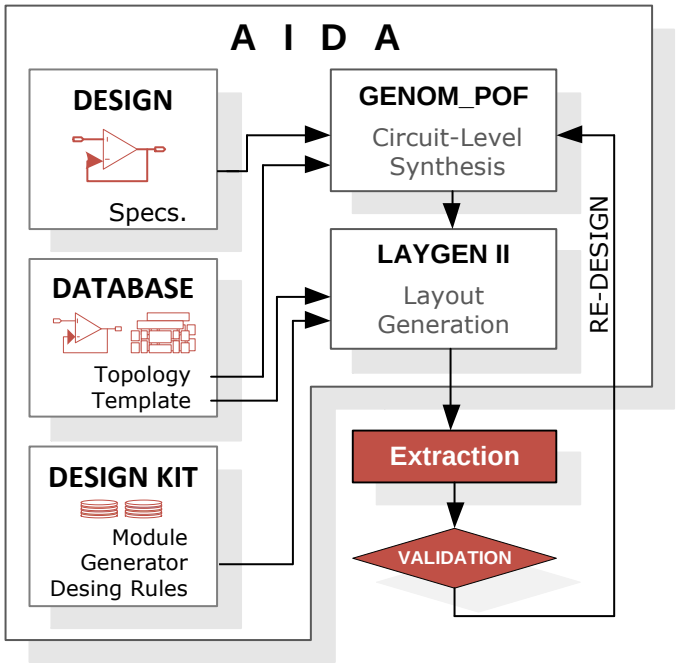

- **SOLUTION ROBUSTNESS**
  - account to extreme variations (CL) - corners validation
  - parametric module generator (LL)
  - multi-objective multi-constraint optimization kernels (CL, LL)
- **DESIGNER INTERFACE**
  - file level (CL)
  - GUI in Java™ (LL)
- **DEGREE of INTEGRATION with Ctools**
  - standard Spice like netlists as entry
  - standard GDSII file as output

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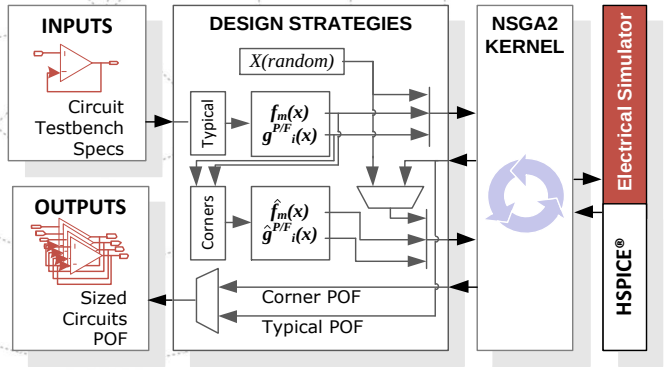
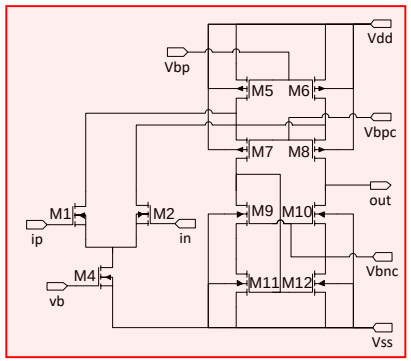
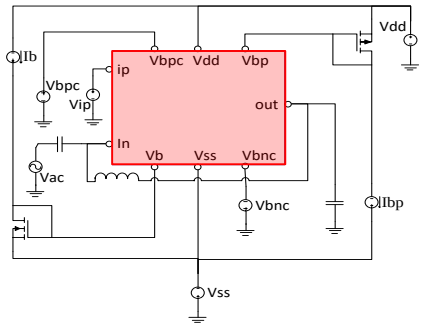
CS1: Circuit-Level Synthesis - GENOM-POF (1 of 3)

Design Specs





single-ended folded cascode amplifier



circuit testbench

Constraints	Measure	Target	Units	Description
Performance	gb	≥ 24	MHz	Unit-gain frequency
	a0	≥ 20	dB	DC Gain
	sr	≥ 10	V/µs	Slew Rate
	pm	55 ≤ pm ≤ 90	°	Phase margin
Functional	ov[1]	≥ 25	mV	Vgs –Vt
	d[1]	≥ 1.15	V/V	(Vds – Vdsat)/Vdsat
	osp	≥ 0.3	V	
	osn	≤ −0.3	V	
Objectives	area	minimize	μm^2	Area
	a0	maximize	dB	DC Gain

[1] The constraint applies to: M1, M4, M5, M7, M9 and M11

Var.	l1, l4, l5, l7, l9, l11	w1, w4, w5, w7, w9, w11	Ib [µA]	cn [V]	cp [V]
Max.	0.80e-6	400.0e-6	500	0.0	0.4
Min.	0.12e-6	0.24e-6	30	-0.4	0.0

The variables l1 and w1 are dimensions of M1 and M2; l4 and w4 of M4; l5 and w5 of M5 and M6; l7 and w7 of M7 and M8; l9 and w9 of M9 and M10; l11 and w11 of M11 and M12.

- **INPUT to CL Synthesis**
  - circuit and testbench description
  - search space definition
    - optimization variable ranges
  - optimization problem definition
    - performance constraints
    - functional constraints
    - objectives

CS1: Circuit-Level Synthesis - GENOM-POF (2 of 3)

Multi-Objective Evolutionary Optimization Kernel

$$\text{find } x \text{ that minimize } f_m(x) \qquad m = 1,2,\ldots M$$
$$\text{subject to } g_j(x) \geq 0 \qquad j = 1,2,\ldots J$$
$$x_i^L \leq x_i \leq x_i^U \qquad i = 1,2,\ldots N$$

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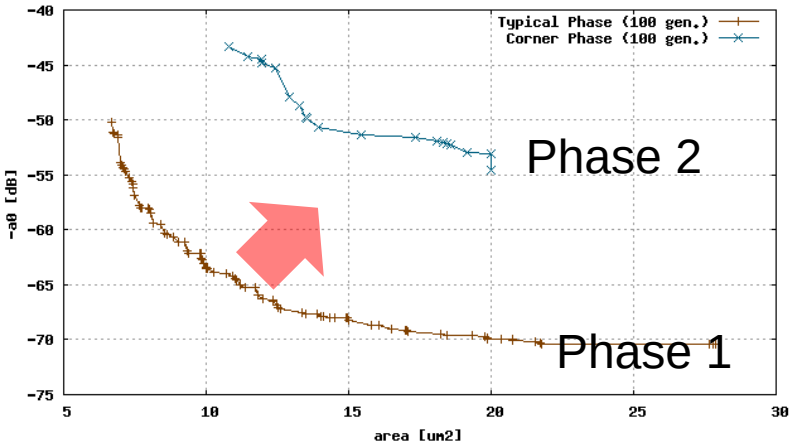
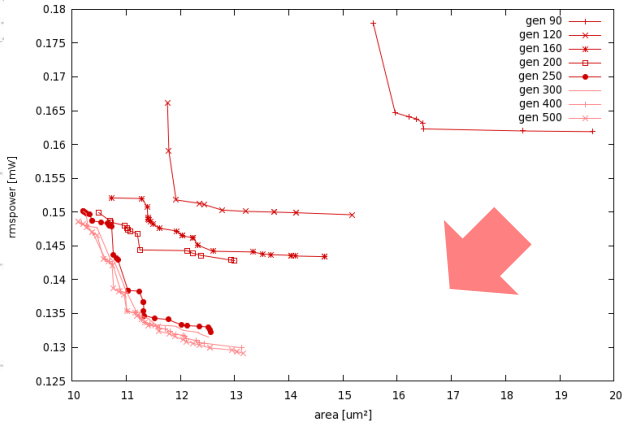
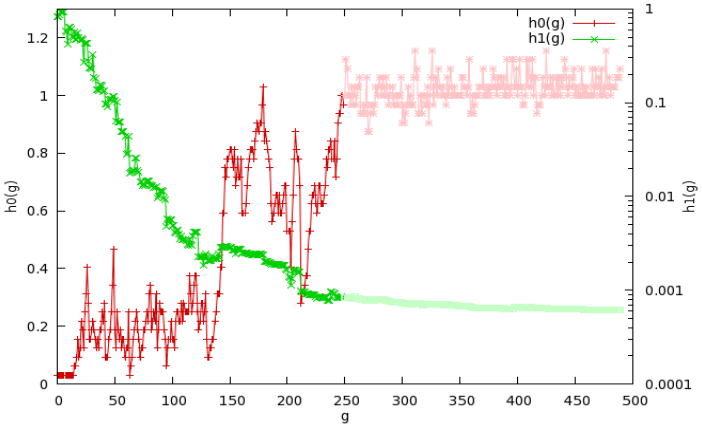


- **Optimization Kernel**
  - Modified NSGA-II
  - **Phase 1**: Typical Optimization
  - **Phase 2**: Corners Optimization
- **POF (Pareto Optimal Front)**
  - Each POF point is a **optimal** sized circuit (Time [s] = **227** (226 sim)!!)

CS1: Circuit-Level Synthesis - GENOM-POF (3 of 3)

Tracking Optimization Process





- **Convergence Measures**
  - POF area
  - number of POF elements
- **NSGA-II Parameters**
  - Population size
  - Crossover
  - Mutation

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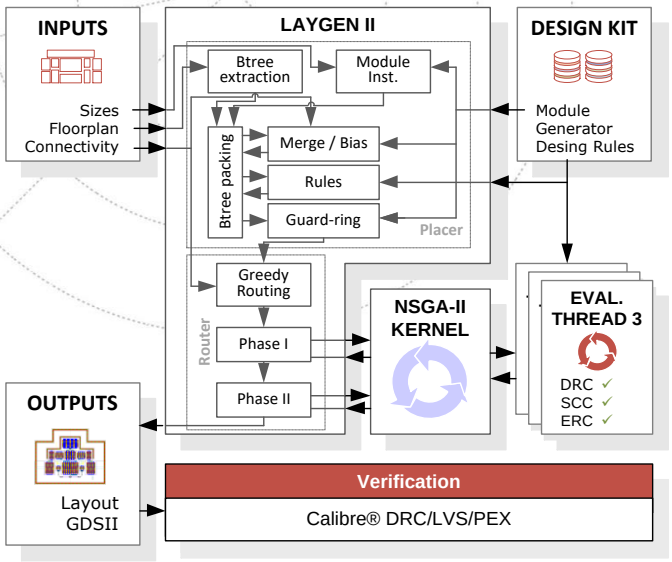
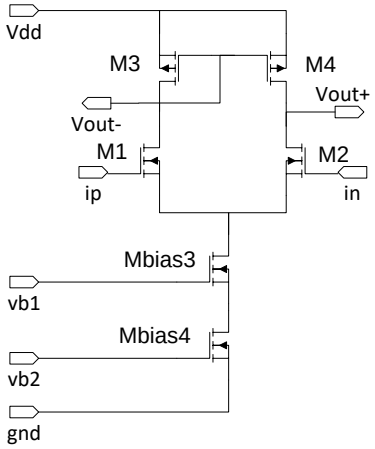
CS2: Layout-Level Synthesis - LAYGEN II

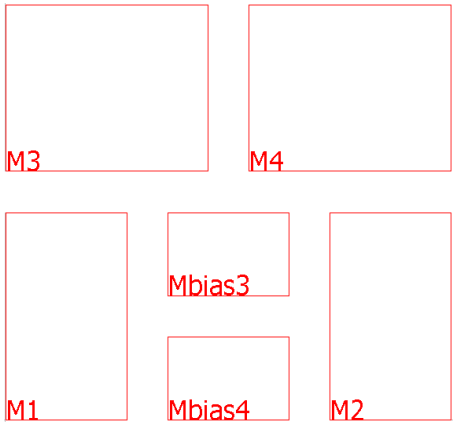
Design Specs



Objectives	Devices	Sizes	
		Width	Length
Estimated Area = 4,7286 μm^2 Power = 1,181 mW DC gain = 30,47 dB	M1, M2	17,6 µm	270 nm
	M3, M4	17,2 µm	350 nm
	Mbias3, Mbias4	3,4 µm	120 nm



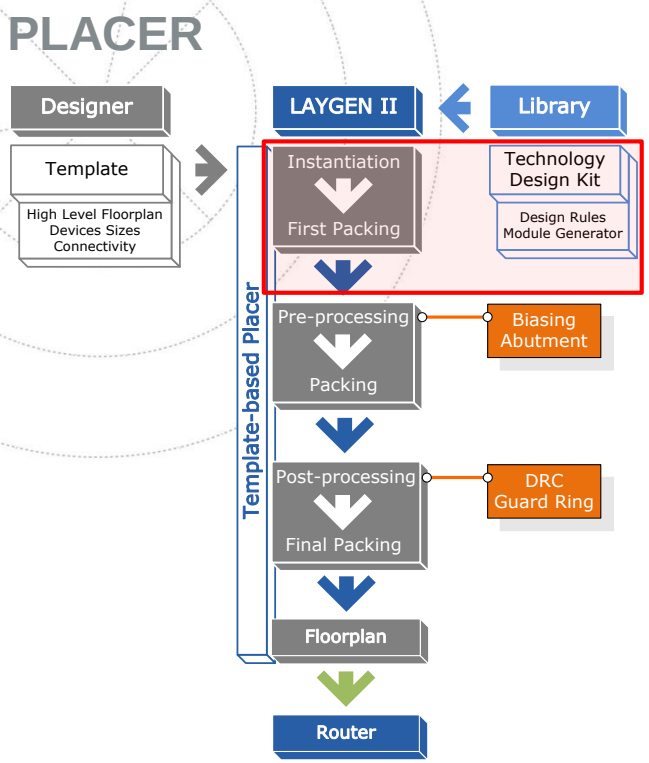
Diff-amp with a current mirror load

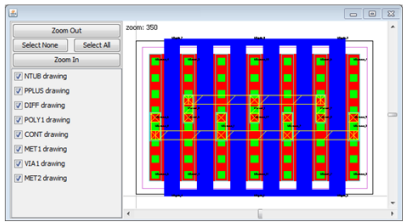


Template view

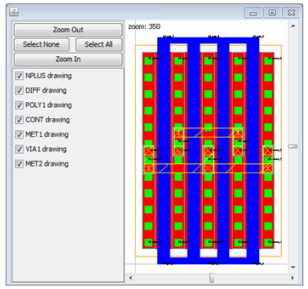
- **INPUT to LL Synthesis**
  - Template description
    - Device Type
    - Relative Placement
  - Device sizes
  - Technology Design Kit **(UMC130nm)**
    - Design Rules
    - Parametric Module Generator

CS2: Layout-Level Synthesis - LAYGEN II

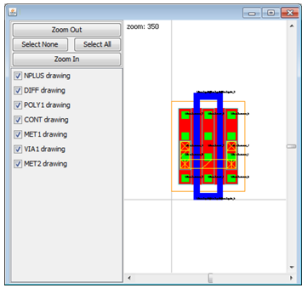




(a) Transistor M3/M4 (W = 17.2 µm, L = 350 nm).



(b) Transistor M1/M2
(W = 17.6 µm, L = 270 nm).

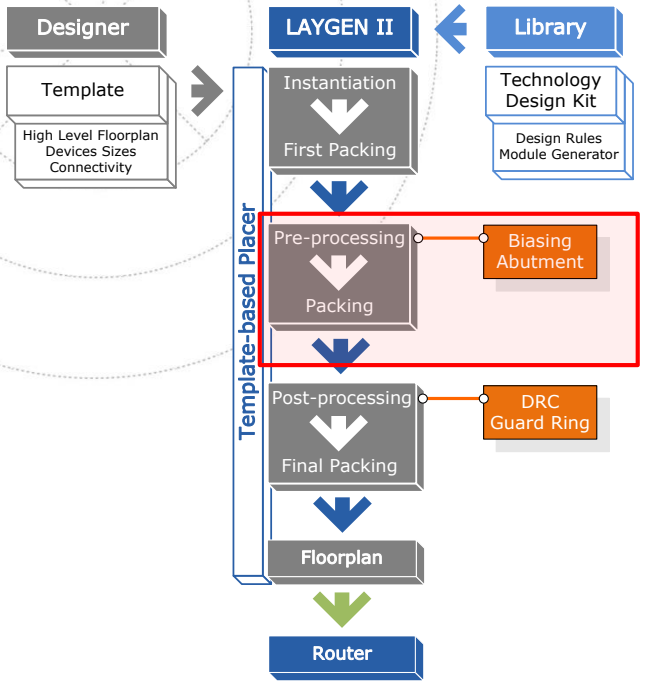


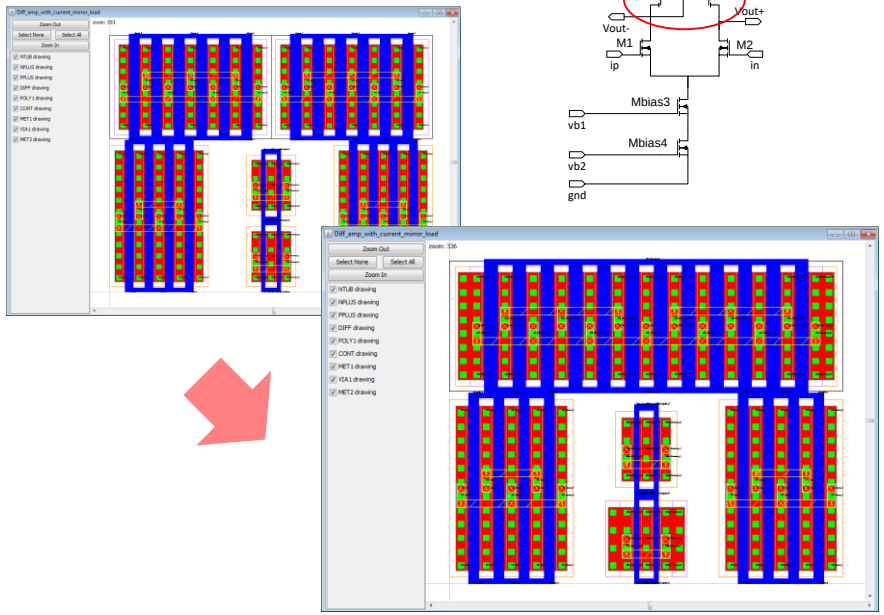
(c) Transistor Mbias3/Mbias4
(W = 3.4 µm, L = 120 nm).

- **Placer**
  - Instantiation - Packing (Phase 1)
    - Device Sizes
    - Module Generator for the target Technology
  - Technology Design Kit

CS2: Layout-Level Synthesis - LAYGEN II

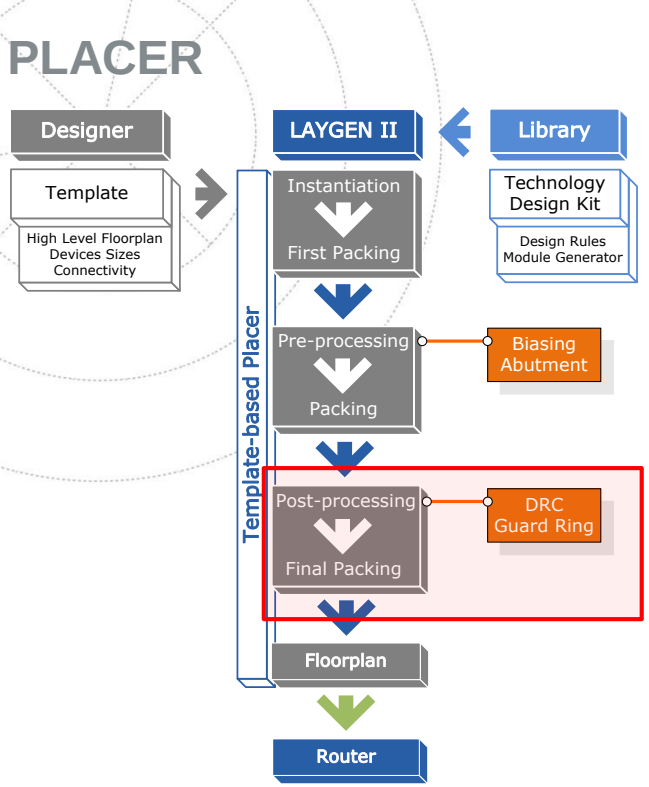
PLACER

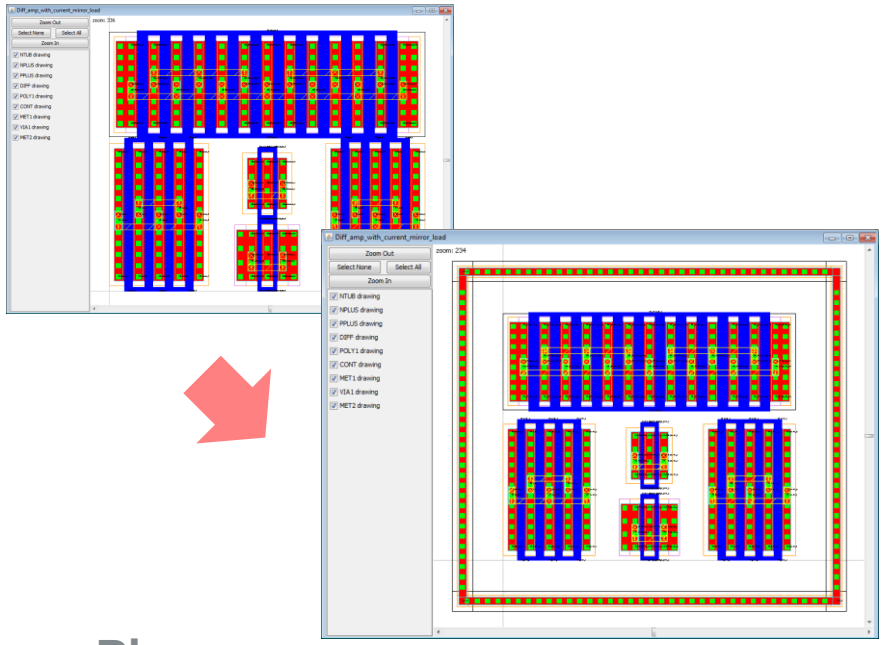




- **Placer**
  - Packing (Phase2)
    - Biasing
    - Abutment
      - Overlapped connection between two cells. Saves space, reduces wiring length, possible parasitics reduction.

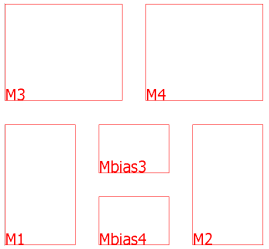
CS2: Layout-Level Synthesis - LAYGEN II



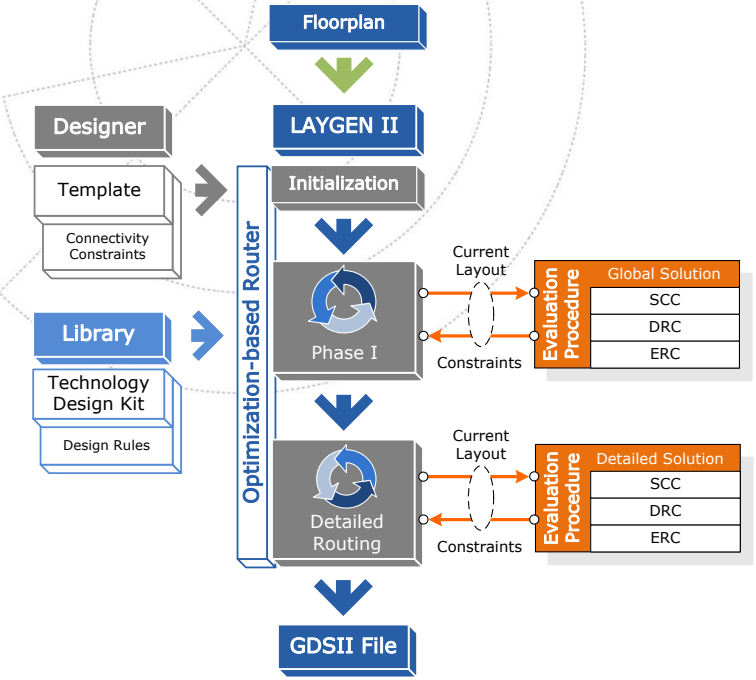


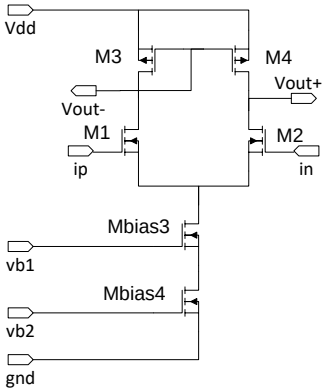
- **Placer**
  - Packing (Phase3)
    - Minimum distances
    - Guard ring
      - Enhanced Immunity against latchup
      - Minimum convex polygon

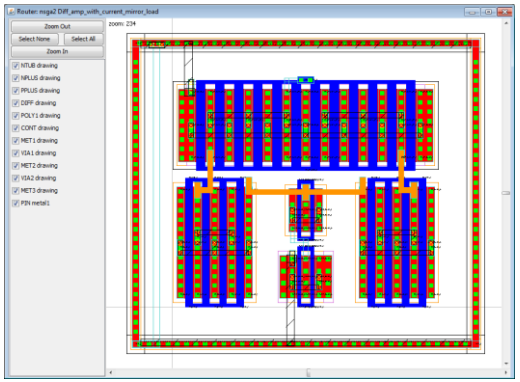
CS2: Layout-Level Synthesis - LAYGEN II



Router







- **Router**
  - Initialization
    - Template (connectivity, symmetry and sensitivity constraints)
  - Optimization (NSGA II Kernel)
    - Built in checkers (DRC – Design Rule Checker; SCC – Short Circuit Checker; ERC – Electric Rule Checker)
    - Phase 1: Global Solution (faster)
    - Phase 2: Detailed Solution (accurate)

Constraint	Target	Description
SCC	= 0	Short circuits.
DRC	= 0	Minimum distance violations.
ERC	= 0	Crossing between noisy and sensitive nets, or running on top of devices.
Objective	**Target**	**Description**
Wiring Lengh	minimize	Total wiring length computed with the associated conductors cost.
Contacts	minimize	Number of contacts or vias used.
Distance	maximize	Distance between noisy and sensititve nets.

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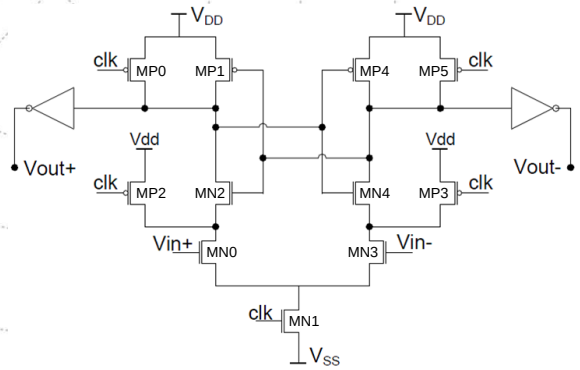
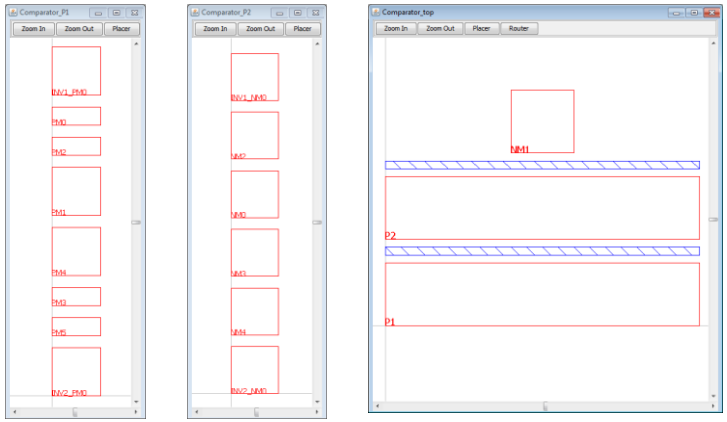
  - Case Studies
- Conclusions

CS: LAYGEN II

Case Study I: Hierarchical Layout Generation



fully-dynamic comparator [Goes et al, 2011]

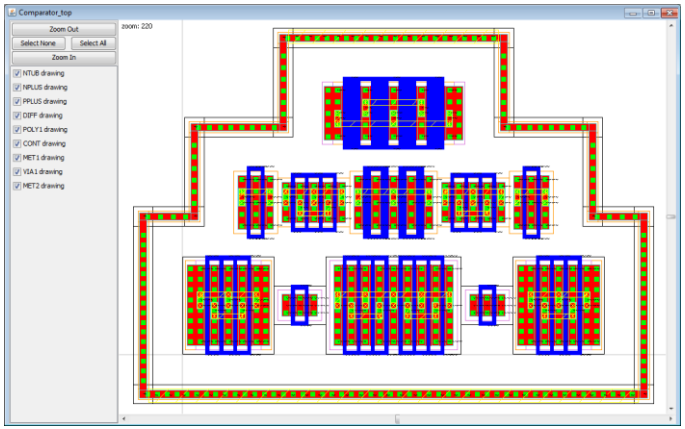


Hierarchical Template Description

device sizes

Devices	Sizes		
	Width	Length	Gates
Inverter MN0	4 µm	120 nm	2
Inverter MP0	12 µm	120 nm	4
MN0, MN3	4 µm	260 nm	2
MN1	8 µm	640 nm	4
MN2, MN4	6 µm	120 nm	4
MP0, MP2, MP3, MP5	820 nm	120 nm	1
MP1, MP4	12 µm	120 nm	4

PLACER



CS: LAYGEN II

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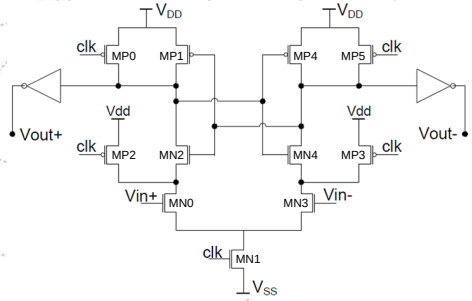

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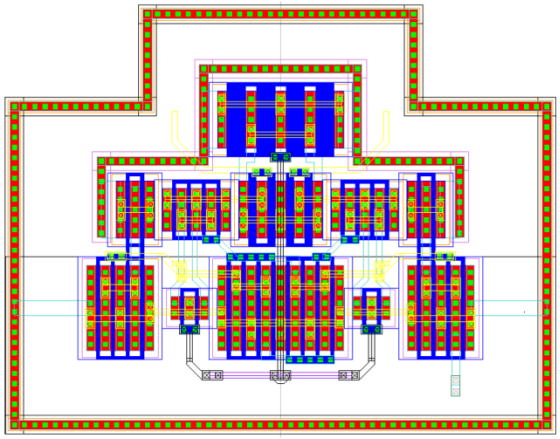
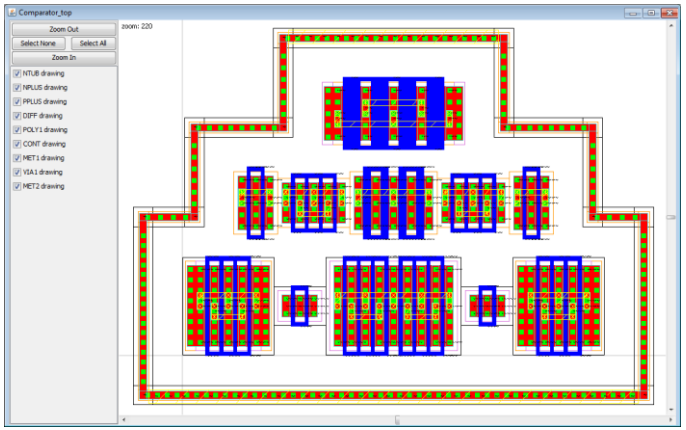
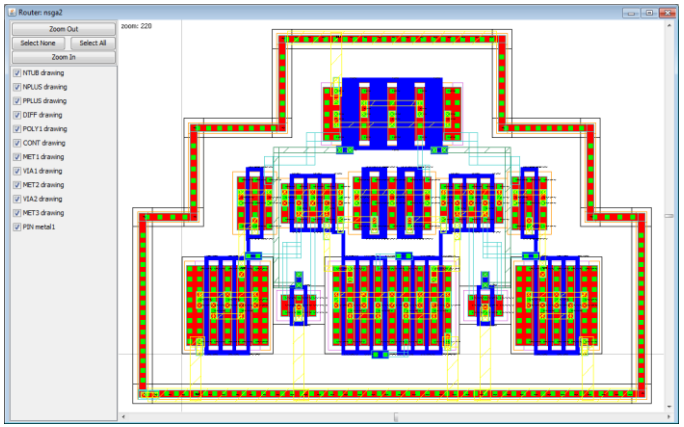


handmade layout [Goes et al, 2011]

PLACER



ROUTER



Template	Placement time	Routing time		Total
		Phase I	Detailed Routing	
Partition 1	83 ms	Not performed.		83 ms
Partition 2	39 ms	Not performed.		39 ms
Top Partition	50 ms	97,571 s	183,286 s	280,907 s

CS: LAYGEN II

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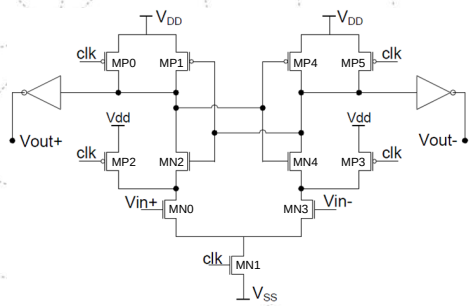

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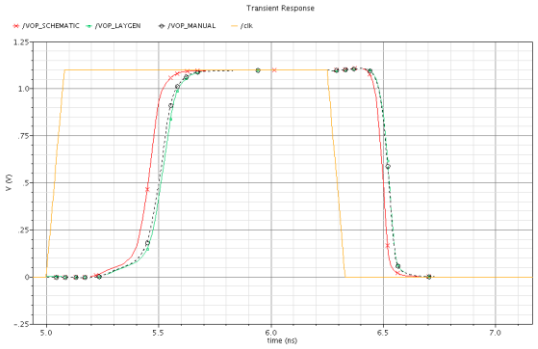
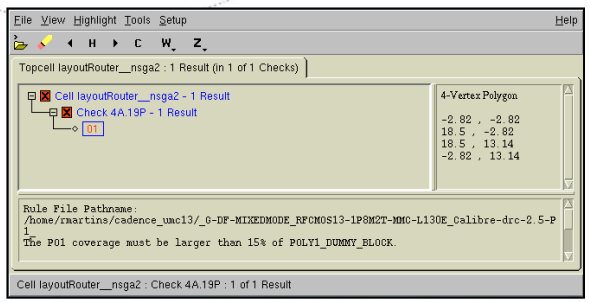
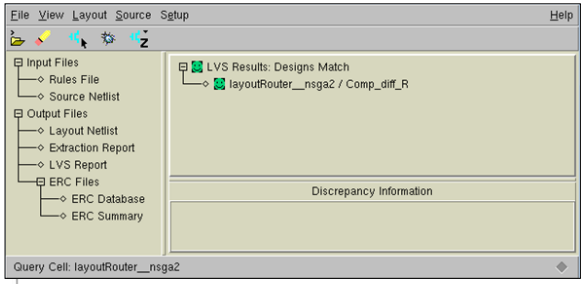
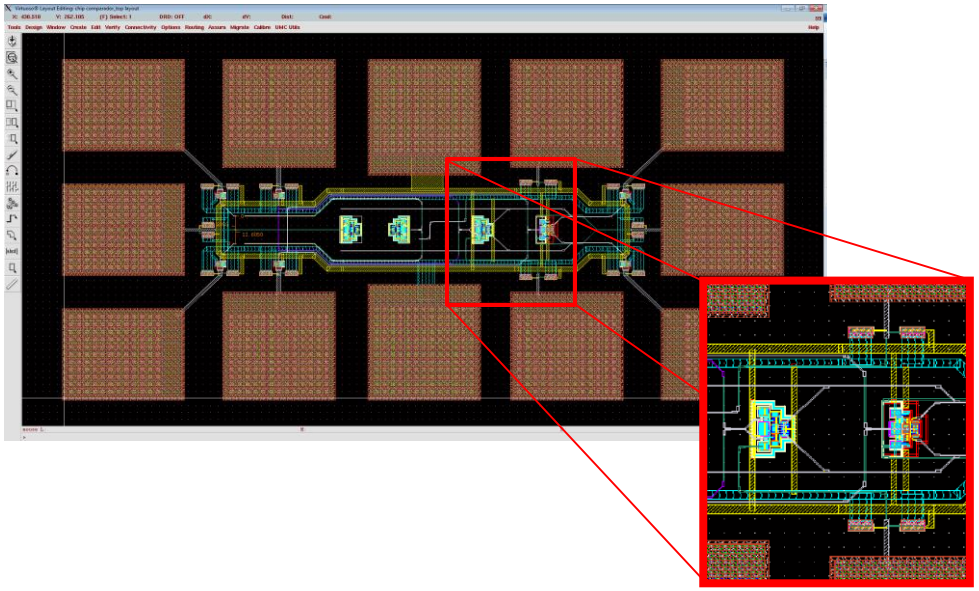


- **Comparator Simulation**
  - Schematic (Red)
  - Handmade (Black)
  - LAYGEN II (Green)

DRC and LVS with CALIBRE®

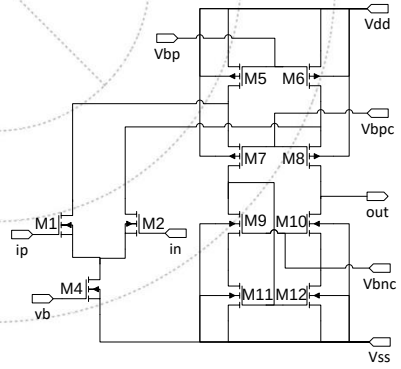




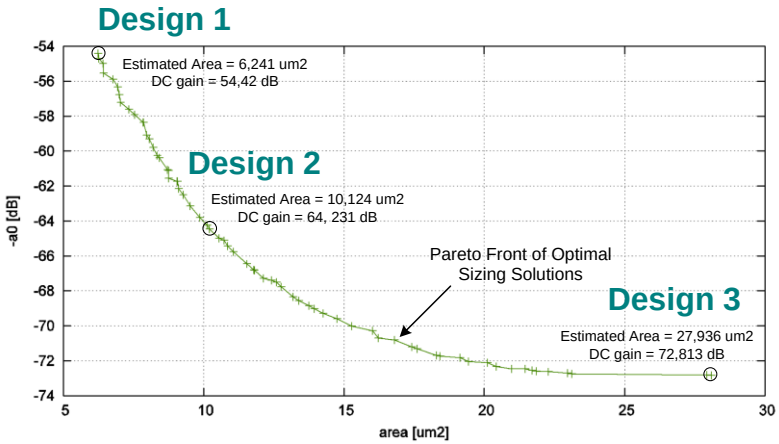


CS: GENOM-POF and LAYGEN II

Case Study II: From Circuit-Level Specs to GDSII Description



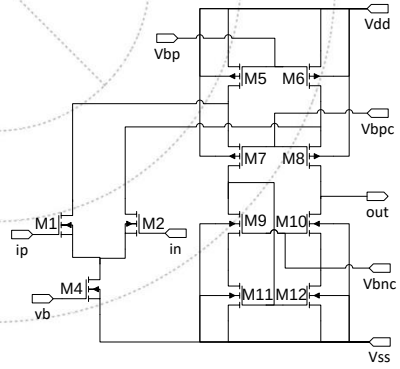
single-ended folded cascode amplifier



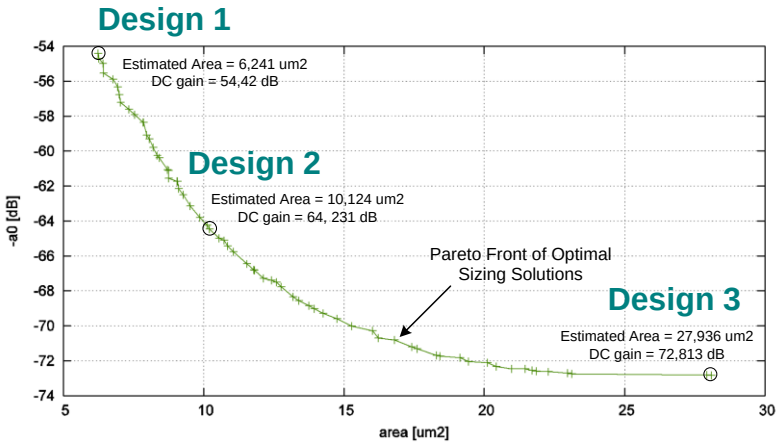
Objectives	Devices	Sizes	
		Width	Length
Design 1 Estimated Area = 6,241 μm^2 DC gain = 54,42 dB	M1, M2	14,67 µm	480 nm
	M4	3,84 µm	530 nm
	M5, M6	13,4 µm	140 nm
	M7, M8	17,77 µm	370 nm
	M9, M10	5,72 µm	310 nm
	M11, M12	2,53 µm	470 nm
Design 2 Estimated Area = 10,124 μm^2 DC gain = 64, 231 dB	M1, M2	13,2 µm	490 nm
	M4	11,33 µm	400 nm
	M5, M6	27,29 µm	290 nm
	M7, M8	36,86 µm	530 nm
	M9, M10	17,61 µm	540 nm
	M11, M12	7,61 µm	730 nm
Design 3 Estimated Area = 27,936 μm^2 DC gain = 72,813 dB	M1, M2	41,22 µm	760 nm
	M4	69,09 µm	670 nm
	M5, M6	153,37 µm	570 nm
	M7, M8	249,84 µm	780 nm
	M9, M10	55,29 µm	790 nm
	M11, M12	12,21 µm	800 nm

CS: GENOM-POF and LAYGEN II

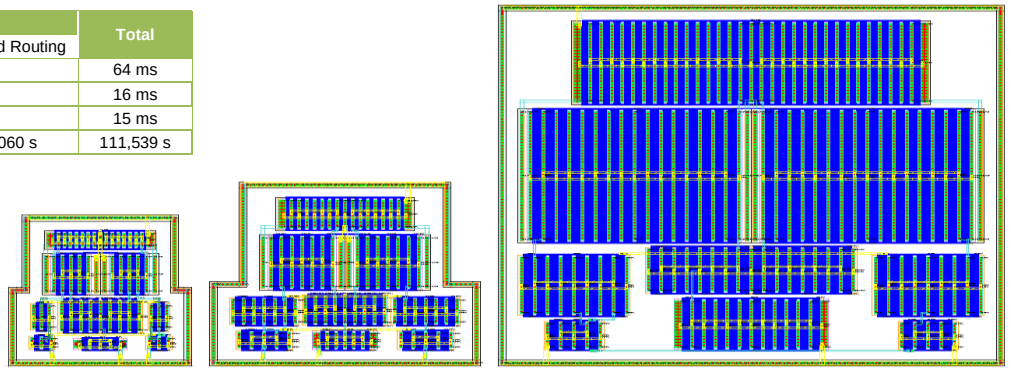
Case Study II: From Circuit-Level Specs to GDSII Description



single-ended folded cascode amplifier



Template	Placement time	Routing time		Total
		Phase I	Detailed Routing	
Partition 1	64 ms	Not performed.		64 ms
Partition 2	16 ms	Not performed.		16 ms
Partition 3	15 ms	Not performed.		15 ms
Top Partition	41 ms	40,438 s	71,060 s	111,539 s



Design 1 Design 2 Design 3

OUTLINE

- Motivation
- Analog IC DA: Overview
- ICG DA Tools and Methods:
  - Circuit-Level Synthesis: GENOM-POF (**N. Lourenço**, N. Horta)
  - Layout-Level Synthesis: LAYGEN II (**R. Martins**, **N. Lourenço**, N. Horta)
- Conclusions

CONCLUSIONS

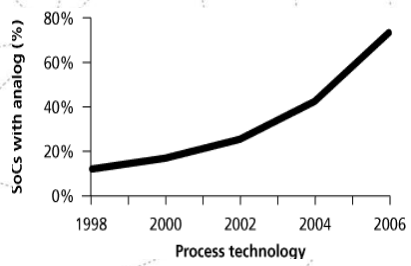
- AIDA, based on GENOM-POF and LAYGEN II, achieves **competitive results with existing SOA solutions** in the area of Analog IC Design Automation
  - @ **Circuit-Level**
    - Multi-objective multi-constrained optimization based on modified NSGA-II optimization kernel
    - High accuracy by implementing an optimization based approach using an electrical simulation as the evaluation engine
    - Robust solution by considering Corners validation
  - @ **Layout-Level**
    - Fast prototyping based on a template based approach and on built-in DRC, SCC, ERC modules.
    - Robust solution by including simultaneously multi-objective optimization together with final validation with CALIBRE® DRC a main reference in the ICs design intended for fabrication.

Future work, mainly, moving to system-level synthesis and deep nanometer technologies.

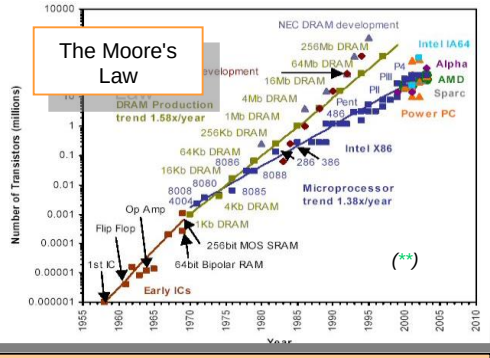
END

MOTIVATION

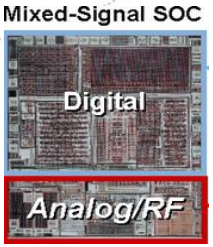
- Electronic Design Automation
  - ICs Market Trends (*)



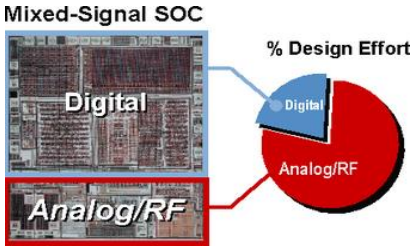
The Moore's Law



  - Integration & Functinalities



  - Analog IC Design Effort



- Constraints
  - \+ PRODUCTIVITY
  - \- PRODUCT DEVELOPMENT CYCLES
  - \- TIME TO MARKET

IC DESIGN AUTOMATION TOOLS

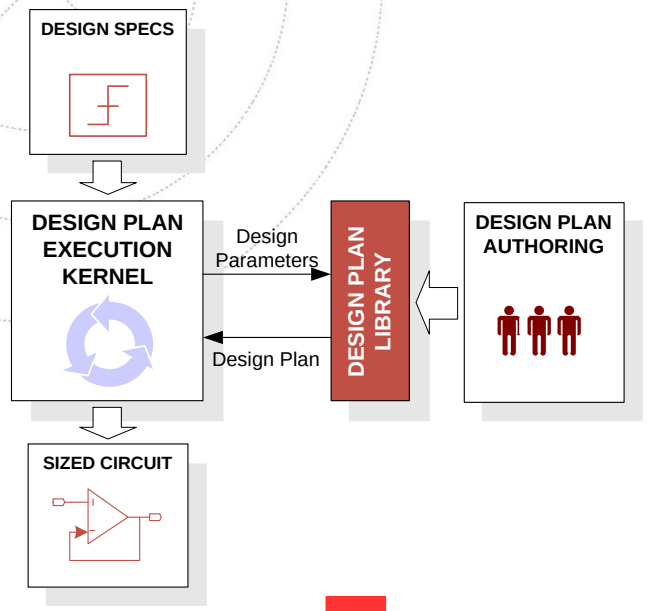
Digital CAD
- ☑ Auto synthesis
- ☑ Auto layout
- ☑ Reuse/IP support

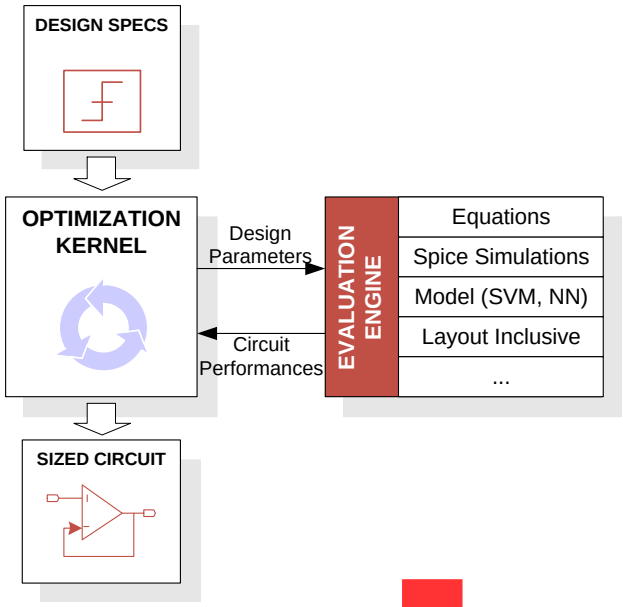
Analog/RF CAD
- ✖ No synthesis
- ✖ No layout
- ✖ No reuse/IP help

(**) *"Exponential Trends in the IC Industries"* - Scotten Jones

ANALOG IC DA: OVERVIEW (CIRCUIT-LEVEL SYNTHESIS)

Knowledge-Based vs Optimization-Based





- Pros and Cons
  - (+) short execution time
  - (-) difficult to scale
  - (-) design plan too complex
  - (-) low accuracy

- Pros and Cons
  - (+) high accuracy, scalable, no need for design plan
  - (-) time consumption

ANALOG IC DA: OVERVIEW (LAYOUT-LEVEL SYNTHESIS)

Optimization-Based, Template-Based and Procedural Approaches

	Layout Tool
Procedural	**ALSYN** [30]; **Jingnan** [31]. (+) Fast processing basic cells; (-) Lack of flexibility, technology migrations force complete cells redesign; high cost of the generation task.
Template	**IPRAIL** [32]; **LAYGEN** [13]; **ALADIN** [33]; **ALG** [34]; **Zhang** [35]. (+) Places modules in a short period of time; higher level than procedural; useful for small adjustments like technology migrations; (-) Still limits the search space; designer must add knowledge.
Optimization	**ILAC** [36]; **KOAN/ANAGRAM II** [37]; **LAYLA** [38]; **Malavasi** [39]; **ALDAC** [40]. (+) Higher level of abstraction; (-) Slow; not always optimal solutions in terms of area and performance.