High Dynamic Range Signal Conversion

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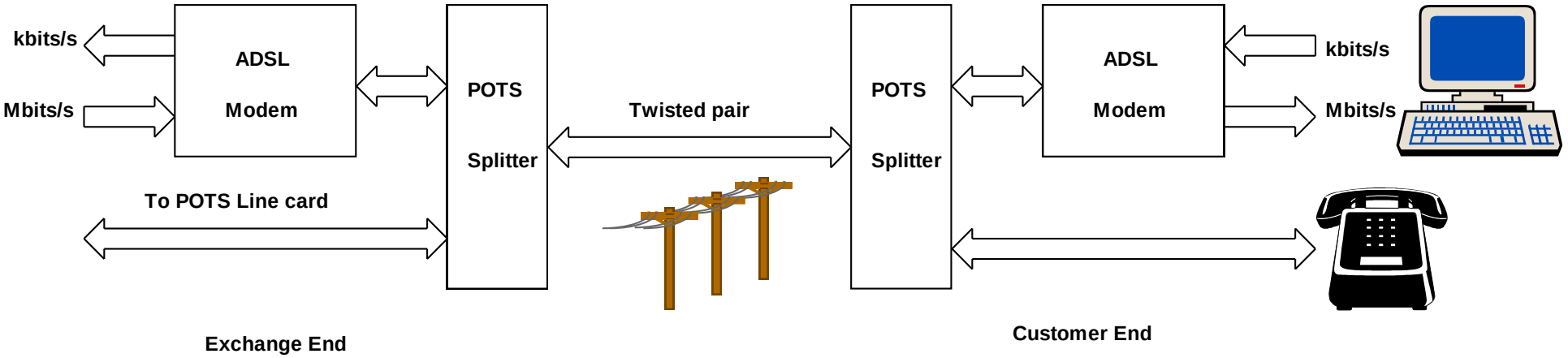
Outline

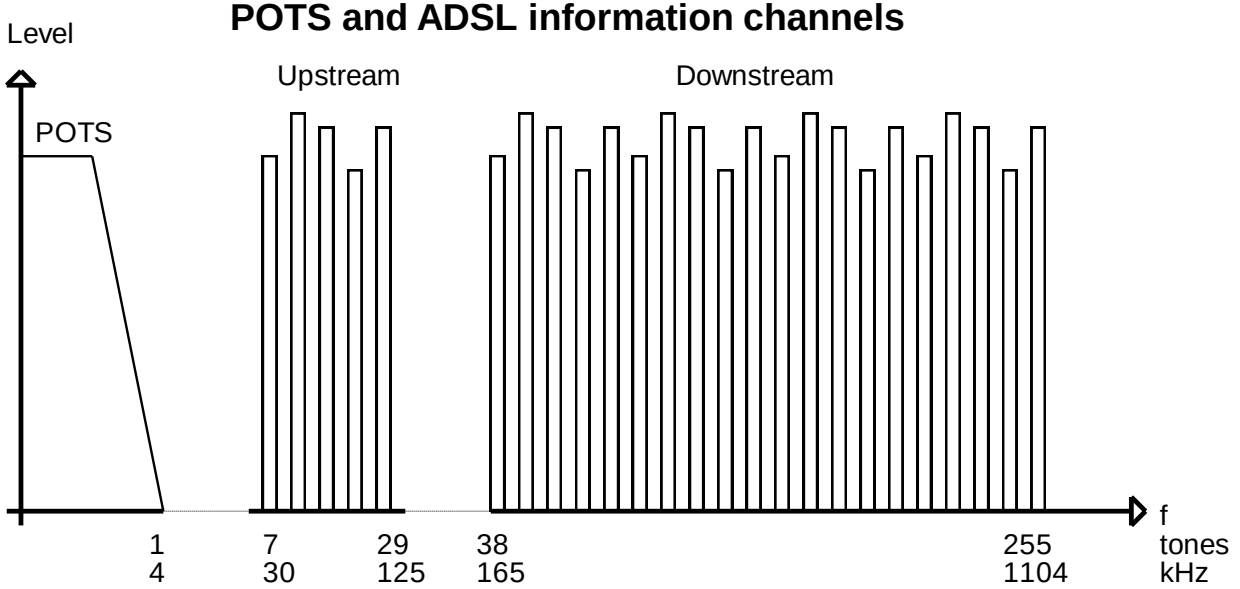
- Context
- Pipeline Architecture
- Design of a 15-bit 10 MS/s Pipeline ADC
- Design of a 9-bit 10MS/s Logarithmic Pipeline ADC
- Other Projects
  - DC-DC controller for Space Applications
  - Class D Audio Amplifier

Context

ADSL modem structure



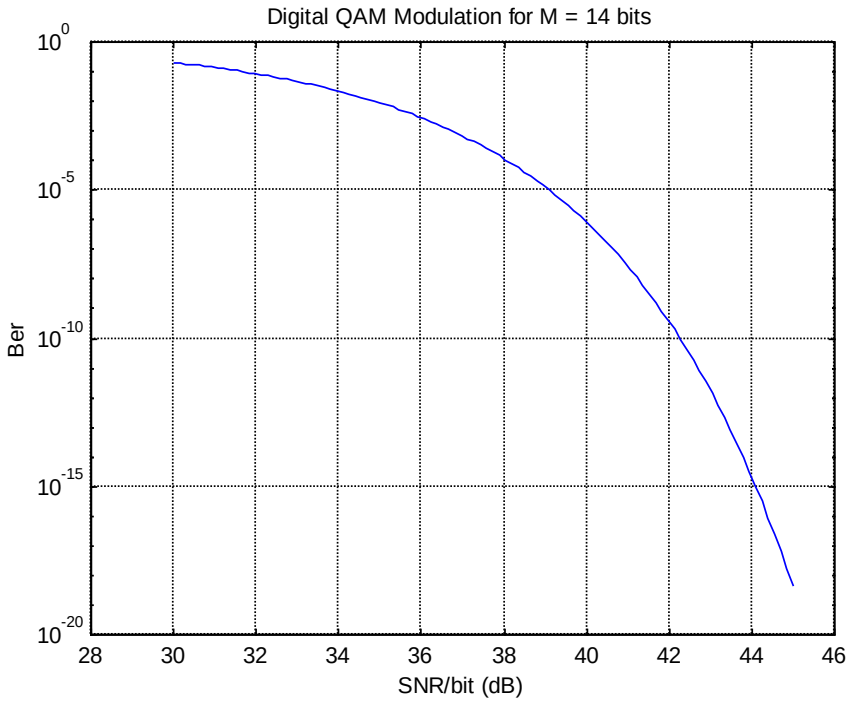
POTS and ADSL information channels



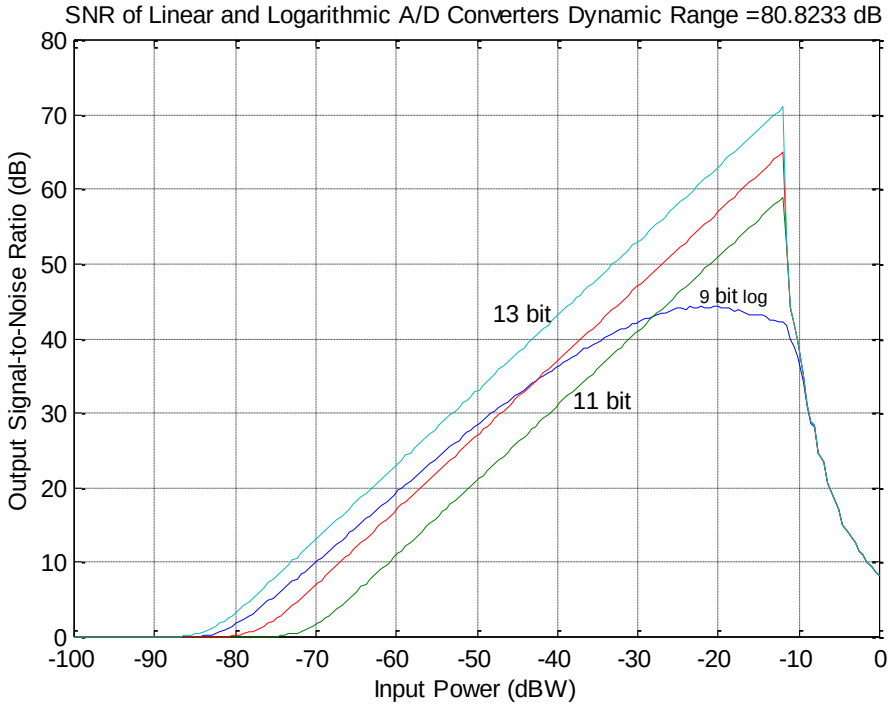
- 255 subcarriers
- 14-bit QAM
- Up to 8.8 Mbit/s

System considerations

Bit error rate probability as a function of SNR for 14 bit QAM



Simulation with white noise

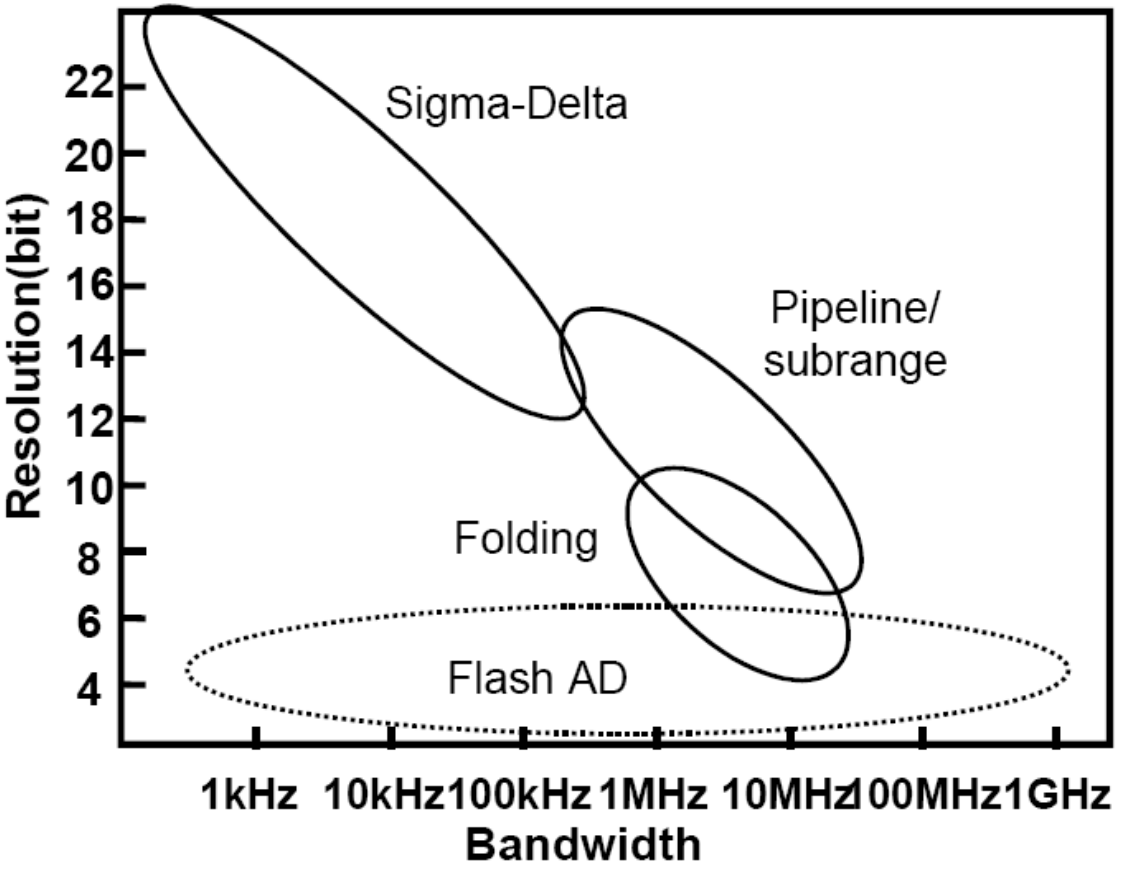


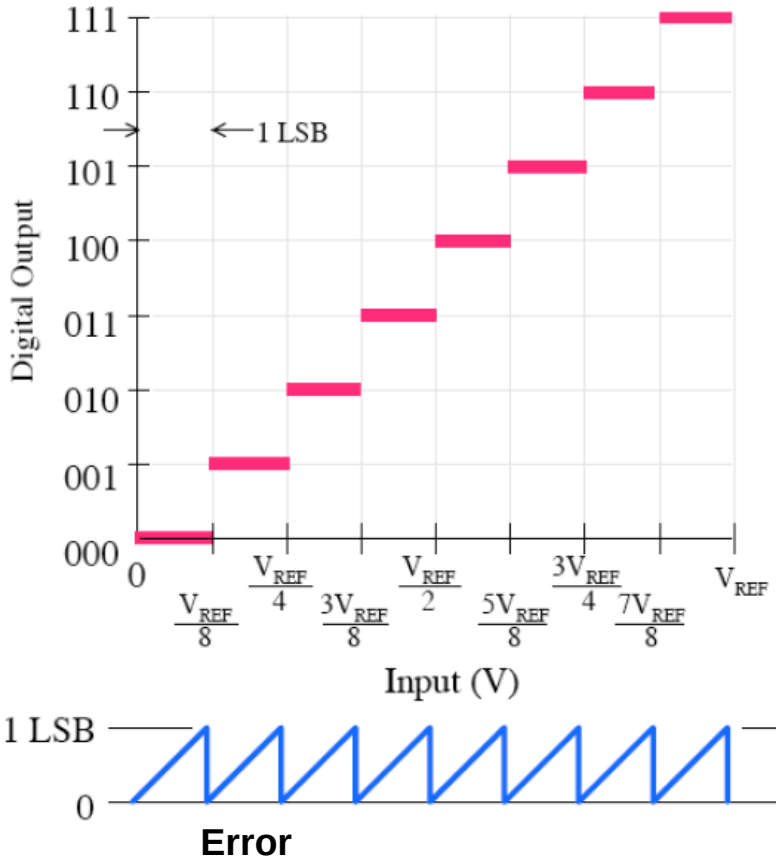
- **For ADSL a ber of 10^{-8} requires an SNR of 42 dB for 14QAM**
- **ADSL requires an 80-dB dynamic range ADC due to signal dynamics**
  (80 dB = 42dB QAM + 3dB margin + 15dB crest factor + 10dB AGC + 10dB crosstalk)

2 solutions ⇒

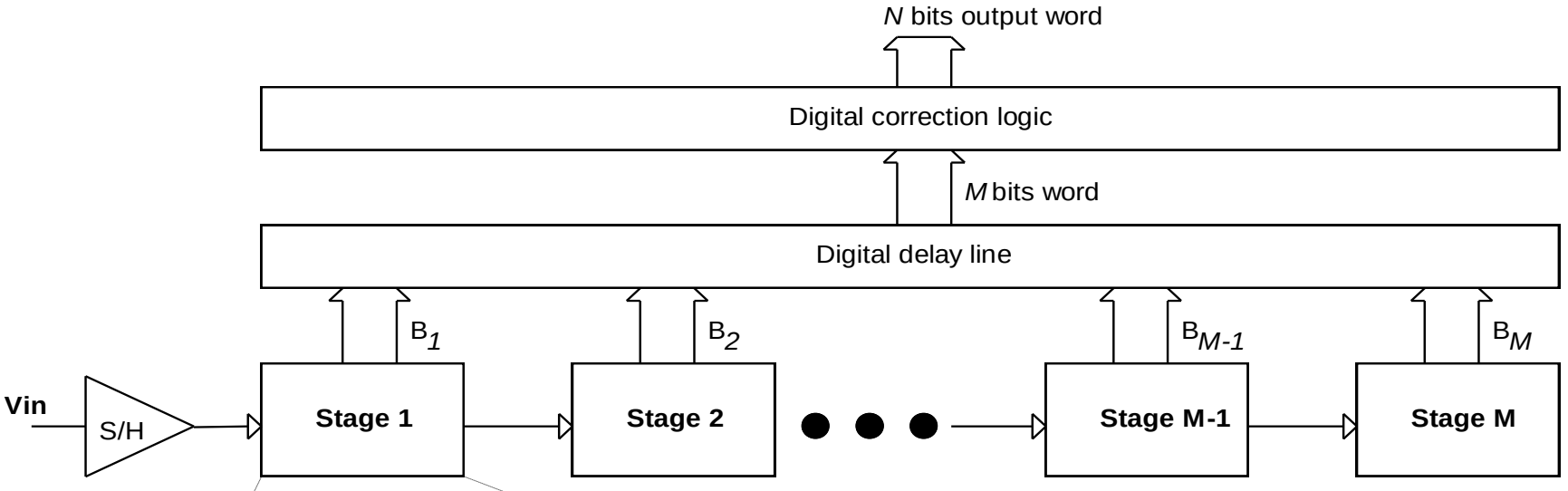
- **Linear pipeline ADC with 13-bit resolution**
- **Logarithmic 9-bit ADC converter with a max SNR of 44.3 dB and 80 dB dynamic range**

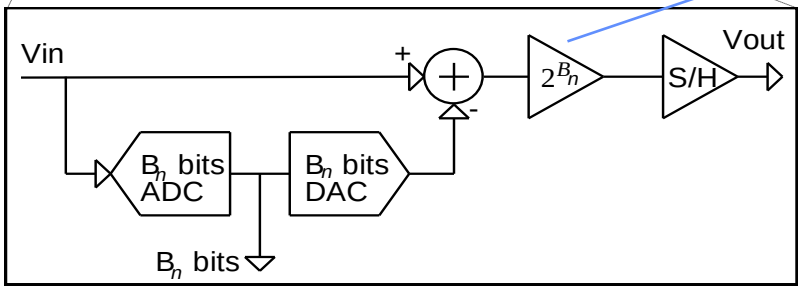
ADC Converter Types





Pipeline ADC

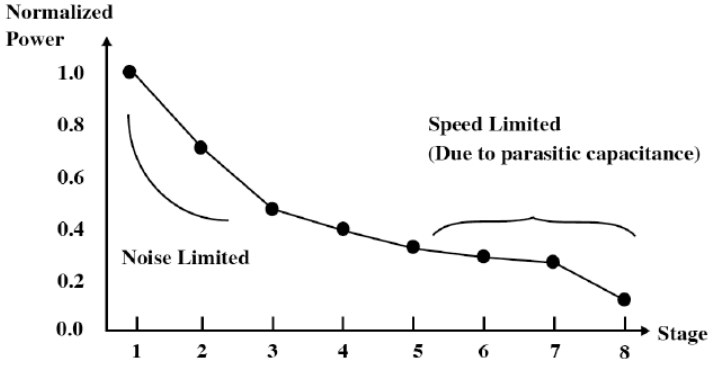




$$A_{OL} > \frac{2^{N+1}}{\beta}$$

$$GBW > \frac{F_{clk}(N+1)\ln 2}{2\pi\beta}$$

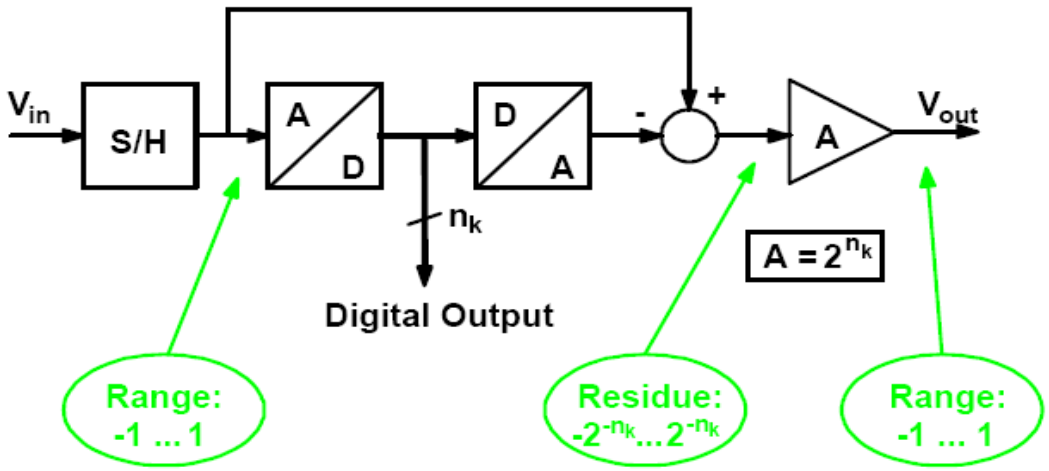
Amplifier specifications

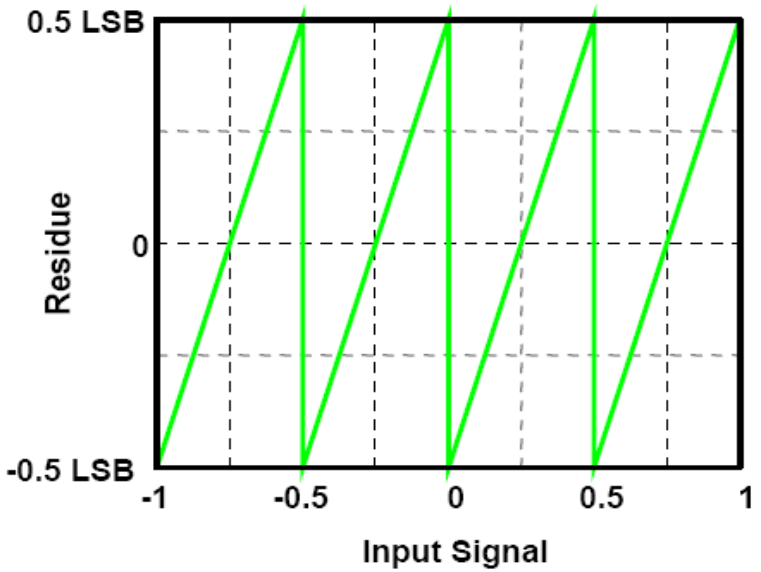


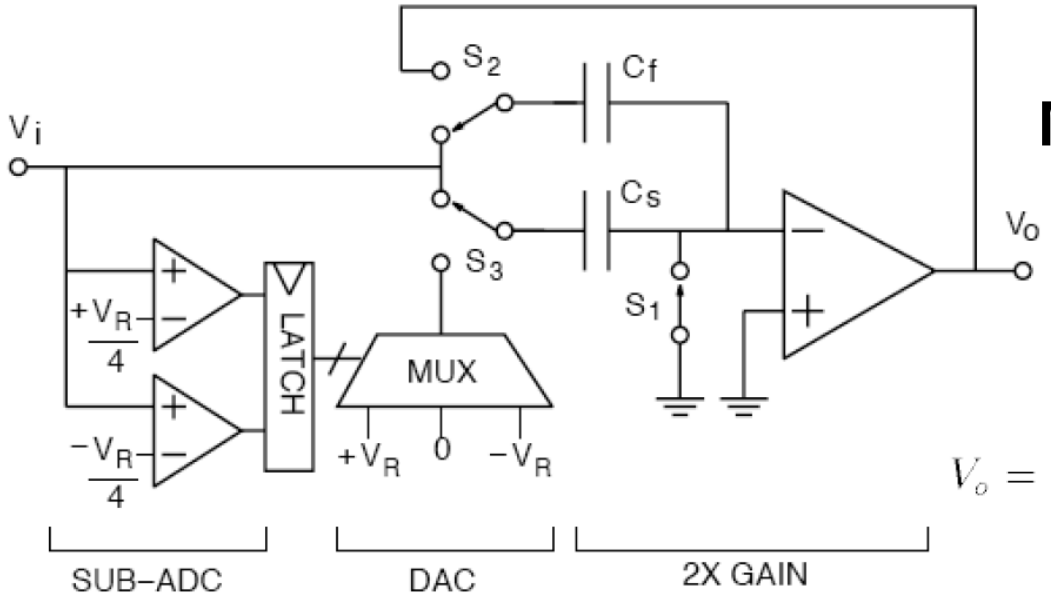
Input Noise

$$V_{ni} = \sqrt{\frac{V_{no,S/H}^2}{1} + \frac{V_{no,Stage1}^2}{G_1^2} + \frac{V_{no,Stage2}^2}{G_1^2 G_2^2} + \cdots \frac{V_{no,Stage(M-1)}^2}{G_1^2 G_2^2 \ldots G_{M-1}^2}}$$

Pipeline ADC







MDAC

$$V_o = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_i - \frac{C_s}{C_f}V_{ref} & \text{if } V_i > V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i & \text{if } -V_{ref}/4 \le V_i \le +V_{ref}/4 \\ \left(1+\frac{C_s}{C_f}\right)V_i + \frac{C_s}{C_f}V_{ref} & \text{if } V_i < -V_{ref}/4 \end{cases}$$

Matlab Pipeline ADC Model

Pipeline ADC Generic Model

Generic ADC Pipeline Model Generator/Evaluator

Simulation Conditions

- [ ] Change Random Seed Alwa...
- [x] Save Results
- [x] Analyse INL/DNL
- [x] Analyse FFT
- [x] Sinusoidal Input
- [ ] Include Front-end Stage Distorti...
- [ ] Ideal Model
  - [ ] Ideal Capacitors
  - [ ] Ideal Opamps DC gain
  - [ ] Ideal Opamps Settling
  - [ ] Ideal Opamps Offset
  - [ ] Ideal Flash Comps Offset
  - [ ] Ideal Flash Comps Sensitivity
  - [ ] Ideal Thermal Noise

Input Signal Atenuation: 0.1 dB Below Full Scale

1 # Monte Carlo Runs

Ploting for Debug

- [ ] Enable Debug Plotting
- [ ] Stg1/SH
- [ ] Stg2
- [ ] Stg3
- [ ] Stg4
- [ ] Stg other
- [ ] Vref Charge Transfer

Pipeline Model Parameters Definition

Model Name	ad1603
Input Vector Break-Down	1
Average Samples per Code	2^3
MDAC FS (Vrefp-Vrefn)	2
Operating Temperature [K]	30+273
Sampling Frequency [Hz]	3e6
Fs/Fi	4
Opamps Slew Rate [V/s]	25000e7
Latch Duration [s]	2e-9
Sampling Random Jitter [s]	0
Noise Integration 0Hz-Fint [Hz]	Fs/2

Create New Model | Lock Model | Load Config. | Run Model | Close All

Validate Input Vector Sizes | Auto Fill Input Vectors

- [x] Use Sample & Hold

ADC Architecture	1 3.5 3.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 2
Unit Capacitors [fF]	2000 1000 250 100 50 50 50 50 50 50 50
Opamp DC Gain [dB]	110 110 75 75 70 60 60 60 60 60 60

Update Noise

- [x] Use Excess Noise Factor Parameter

Stgs ONoise Z [uV]	5 393.3 541 737.3 737.3 737.3 737.3 737.3 737.3 737.3 708.4
Stgs ONoise XY [uV]	5 393.3 541 737.3 737.3 737.3 737.3 737.3 737.3 737.3 708.4
XS Noise Factor Z	1 1 1 3 3 3 3 3 3 3 3
XS Noise Factor XY	1 1 1 3 3 3 3 3 3 3 3
Opamp Offset [mV]	0 0 0 0 0 0 0 0 0 0 0
Comps Offset [V]	7/16 Vref/16 Vref/16 Vref/16 Vref/16 Vref/16 Vref/16 Vref/16
Comps Noise [V]	0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005
Stages Settling Precision [bit]	16 16 14 12 12 8 8 8 8 8 8

Distortion Parameters

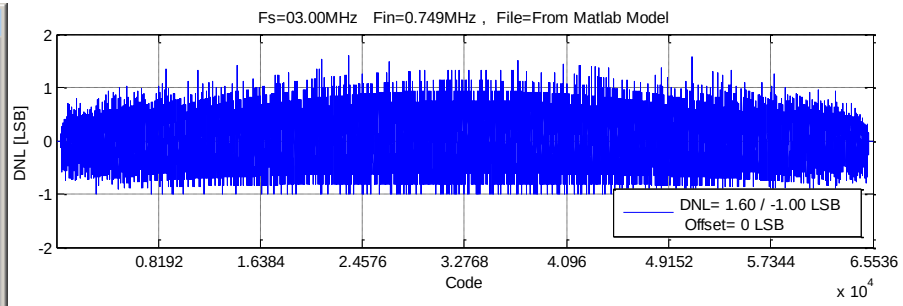
HD2 [dB]	-100
HD3 [dB]	-75
HD4 [dB]	-100
HD5 [dB]	-80
HD6 [dB]	-100
HD7 [dB]	-90

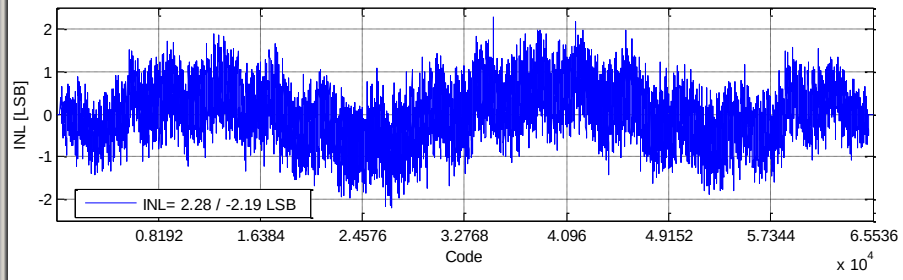
Capacitor Mismatch Info

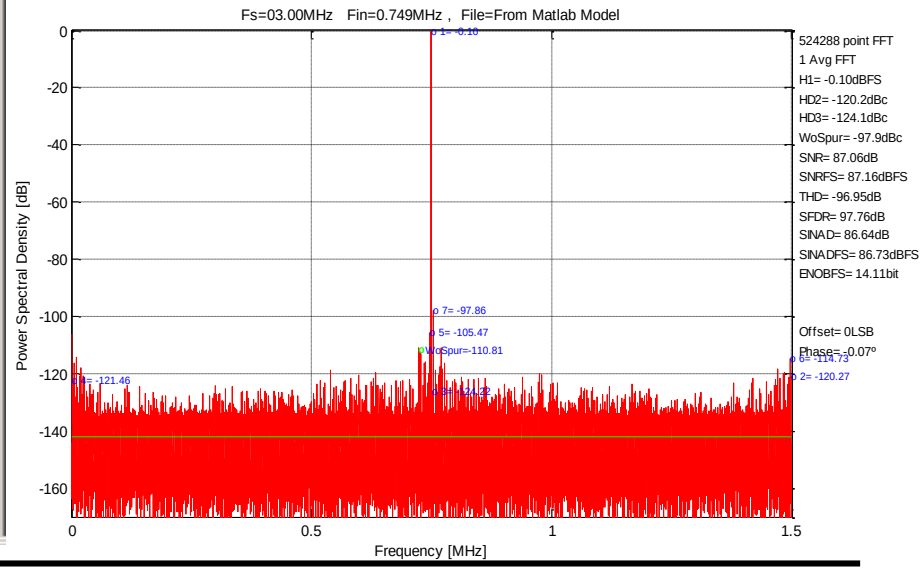
Cap Density vertical (Ca)	0.69e-15
Perimeter cap density (Cp)	0.15e-15
Capacitors area (Caparea)	((sqrt(16*Cp^2+4*Ca.*Cunit)-4*Cp)/(2*Ca)).^
Estimated Cap Density (CapParea)	Ca+Cp
Capacitor Sigma(deltaC/C)	0.805./(sqrt(2*Caparea)*100)

Model Path: E:\Linux\CAD\Projects\CCDAFE01\ESA_CCDAFE01\Docs\Architecture_Analysis\Matlab_model

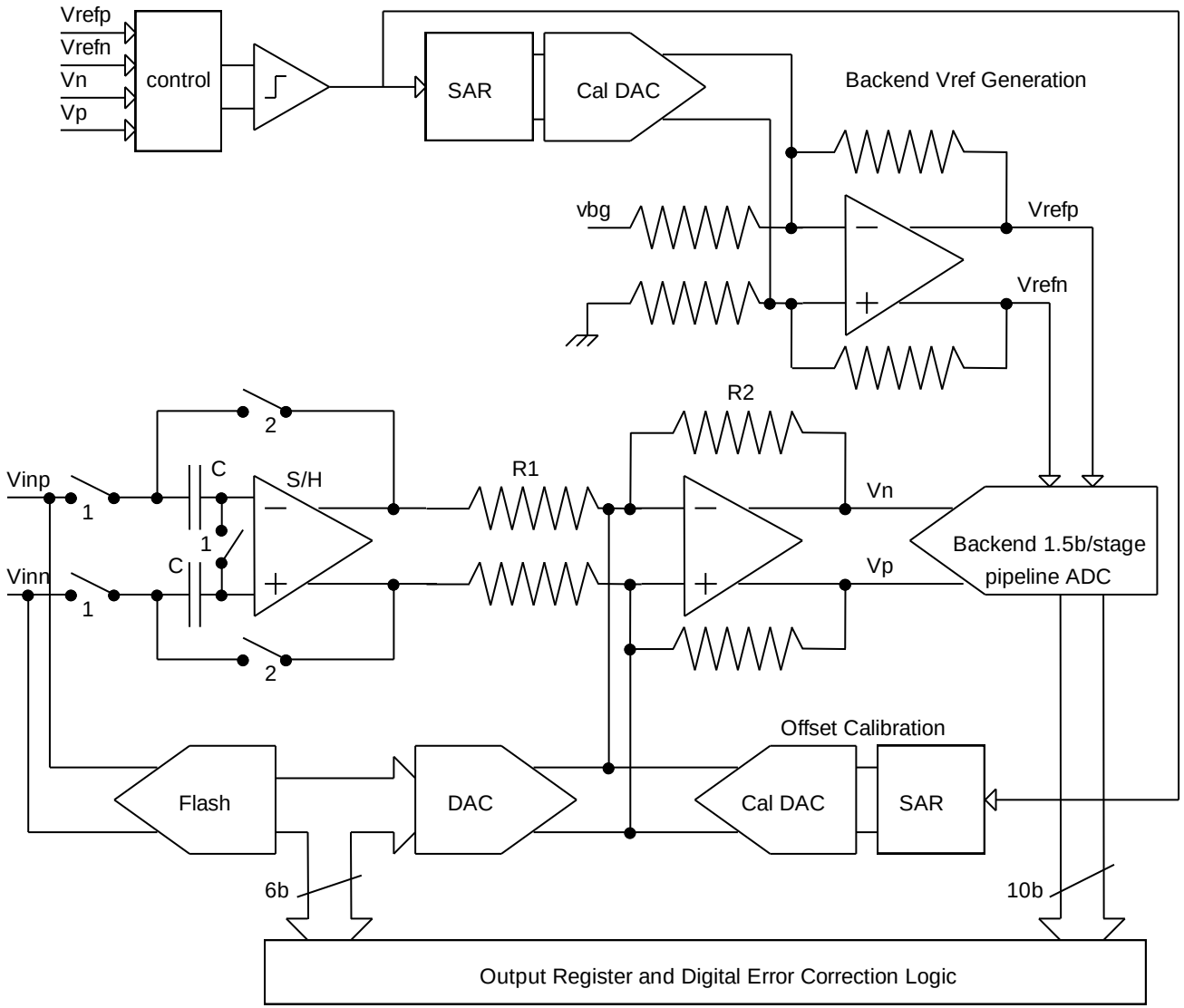
```
.
..
NOT_USED
Used_to_test_functions
adc3v1
```



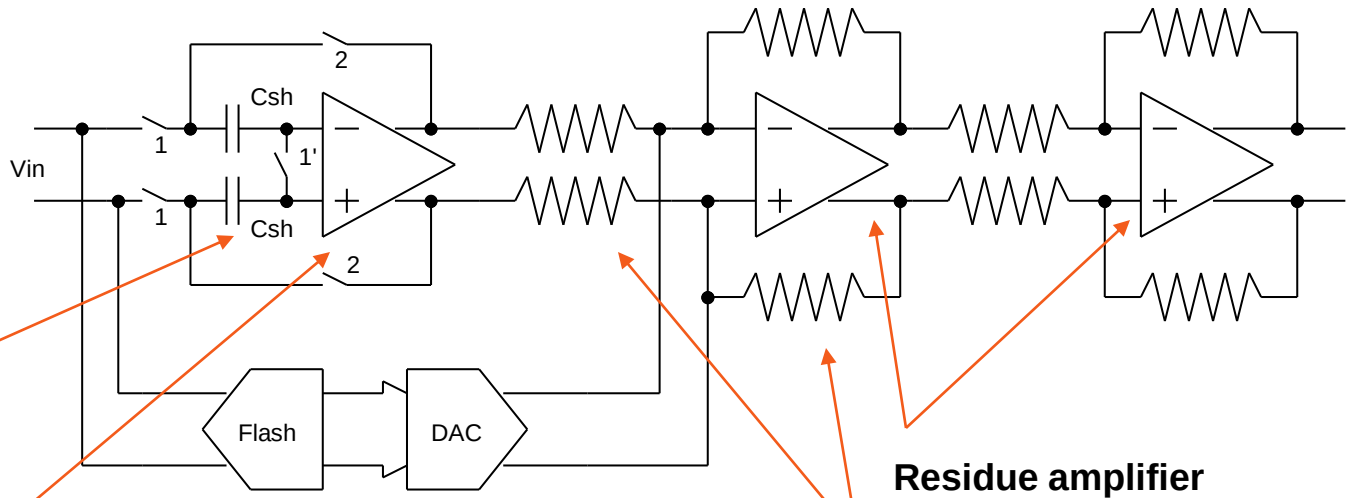




Architecture of the 15-bit 10MS/s self-calibrated pipeline ADC



Noise contribution of the Front-end Pipeline Blocks



Input sampling capacitors

S/H amplifier

DAC

Residue amplifier

Resistors

$$Vndac = \sqrt{\frac{16 \cdot K \cdot T \cdot Id \cdot Fn}{3 \cdot Vod}} \cdot R$$

$$Vnamp = \sqrt{\frac{2}{3}\frac{K \cdot T}{Cc} \cdot \frac{1 + \frac{Vdsat1}{Vdsat7}}{f}}$$ **Kelvin 1998**

The resistors and the DAC inject large noise!

The DAC noise current is proportional to *gm*

$$Vr = \sqrt{4 \cdot K \cdot T \cdot Fn \cdot R} \qquad Fn = \frac{\pi}{2} \cdot Fo = 70MHz$$

SNR system calculation

$$SNR = 10 \cdot \log \left(\frac{\frac{1}{2} \cdot \left(\frac{Vref}{2} \right)^2}{\frac{Vref^2}{12.2^{2N}} + \frac{2 \cdot K \cdot T}{C} + 4 \cdot Vnamp^2 + 2.Vr^2 + 2.Vndac^2 + \frac{2.Vr^2 + 2.Vnamp^2}{32}} \right) \approx 79dB$$

Noise distribution by block

Quantization	**≅ 26%**
KT/C	**≅ 17%**
Resistors	**≅ 20%**
DAC	**≅ 16%**
Amplifiers	**≅ 21%**

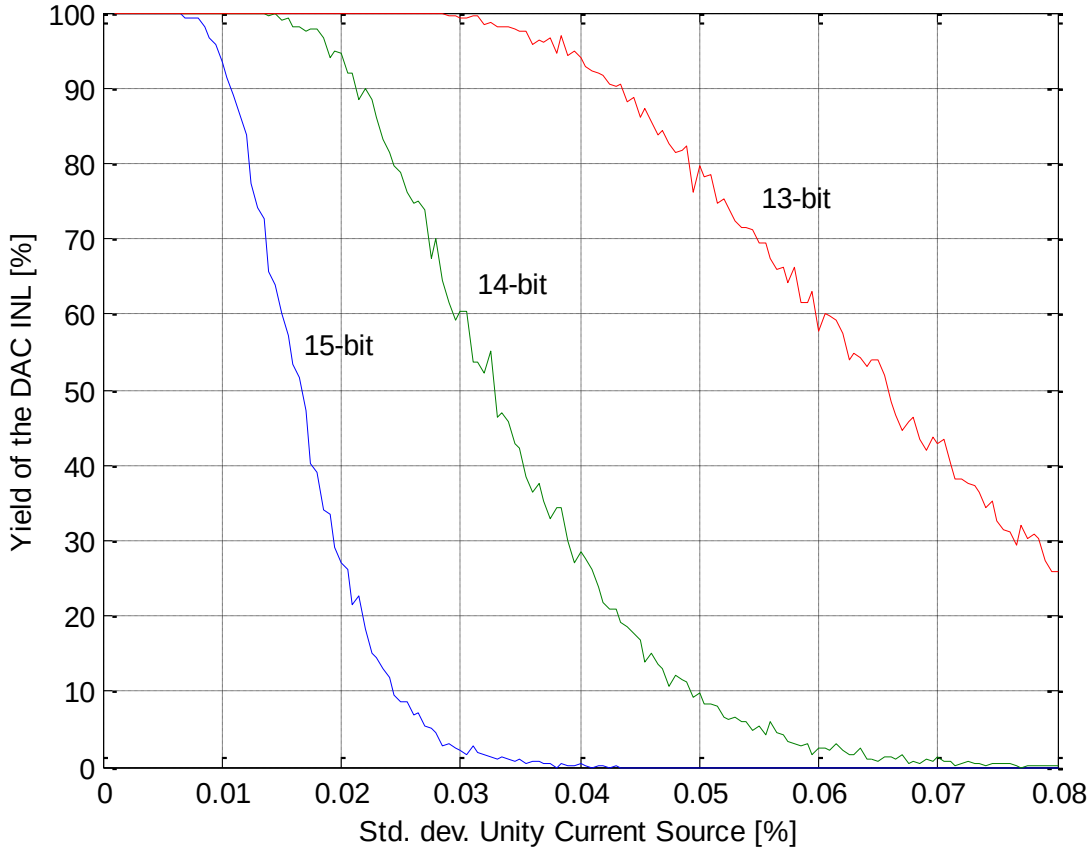
Trade off between power, noise and resolution obtained by program

***C* = 10 pF**
***Cc* = 10 pF**
***Idac* = 1mA**
***Rstring* = 1000 ohm**

Noise Bandwidth of a 2 pole system = 0.7854 Fo helps reducing the noise from the DAC and resistors

Current Steering DAC

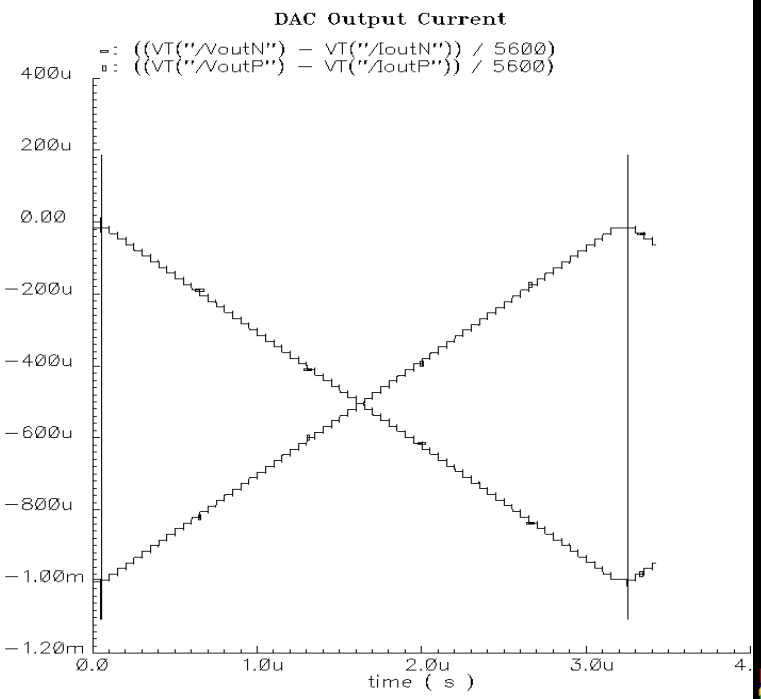
- Current steering DAC requirements: random errors
  - Current source sizing: std dev(ΔI/I) = 0.027% for 13 bit linearity
  - Vod = 0.76V ==> total current source DAC transistor area = 0.817 mm^2 , DAC area = 1.7 mm^2
  - Hierarchical symmetrical switching scheme used to compensate systematic errors



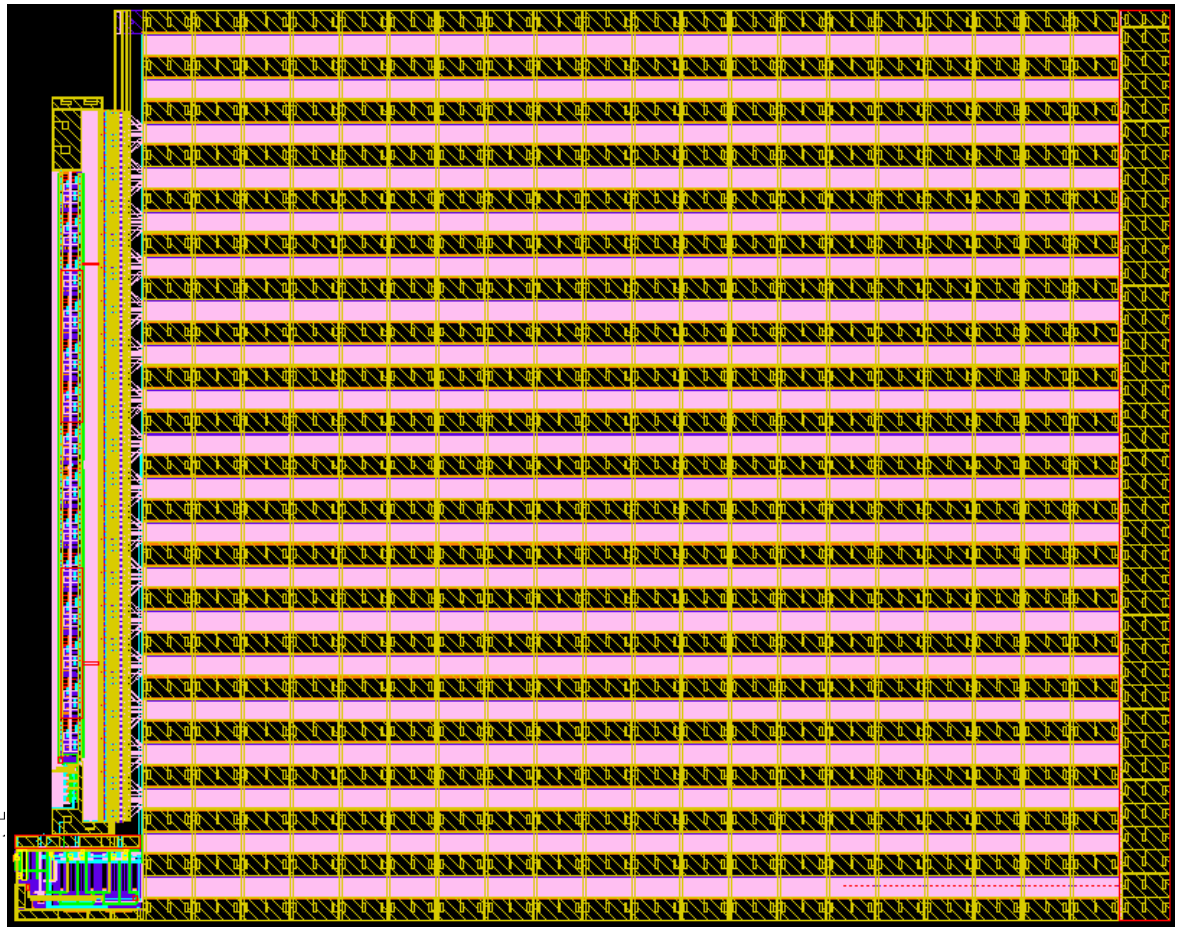
$$(WL)_{\min} = \frac{1}{2}\frac{A_\beta^2 + 4\frac{A_{vt}^2}{V_{ovd}^2}}{\sigma^2\left(\frac{\Delta I}{I}\right)}$$

Current Steering DAC

DAC Output



DAC Layout

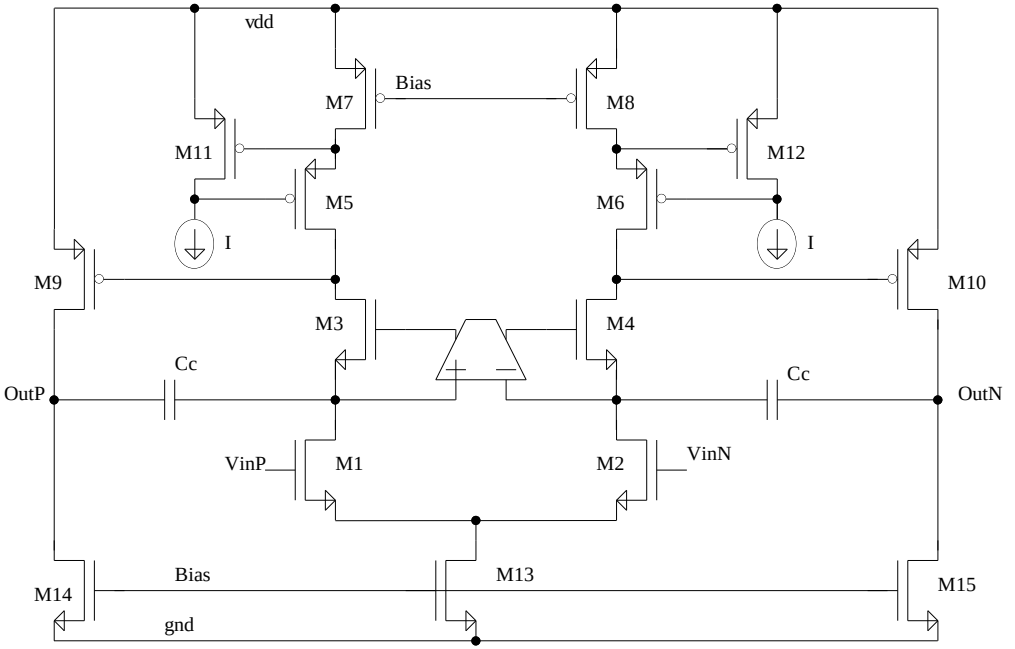


Area = 1.51x1.82 mm²

Residue amplifier

Main schematic of the amplifiers used in the S/H and residue amplifiers

- The amplifiers where designed based on the noise allowed to it dependent on *Cc*
- A telescopic cascode compensation topology was chosen to minimize power
- From *Cc* and *GBW* we obtained the *gm* and current of the input diferential pair



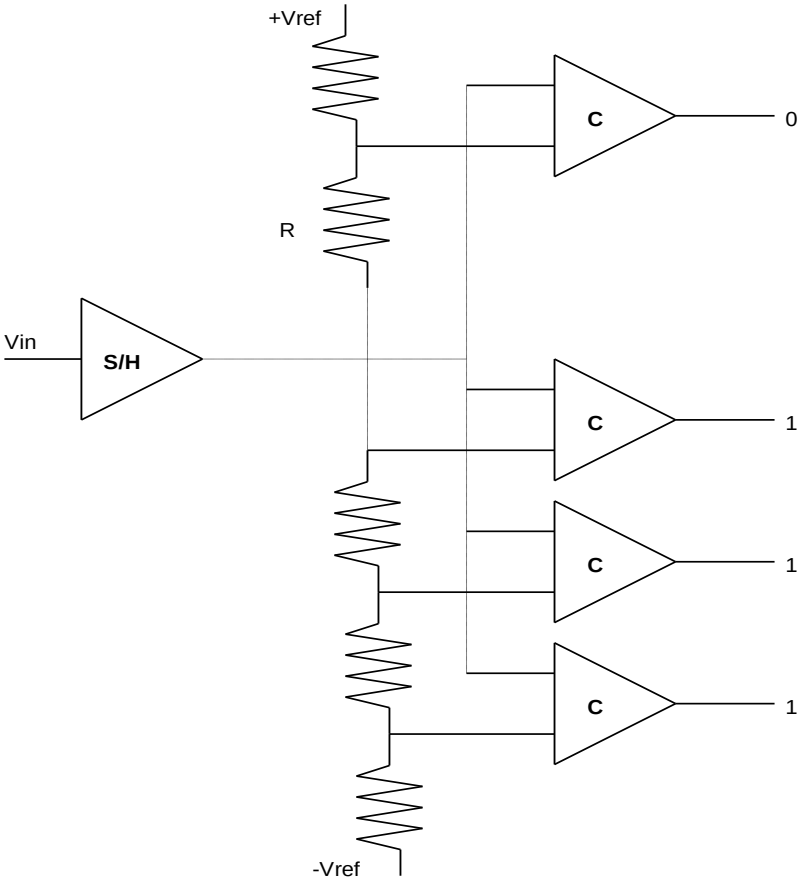
$$GBW = \frac{gm}{2\pi C_C}$$

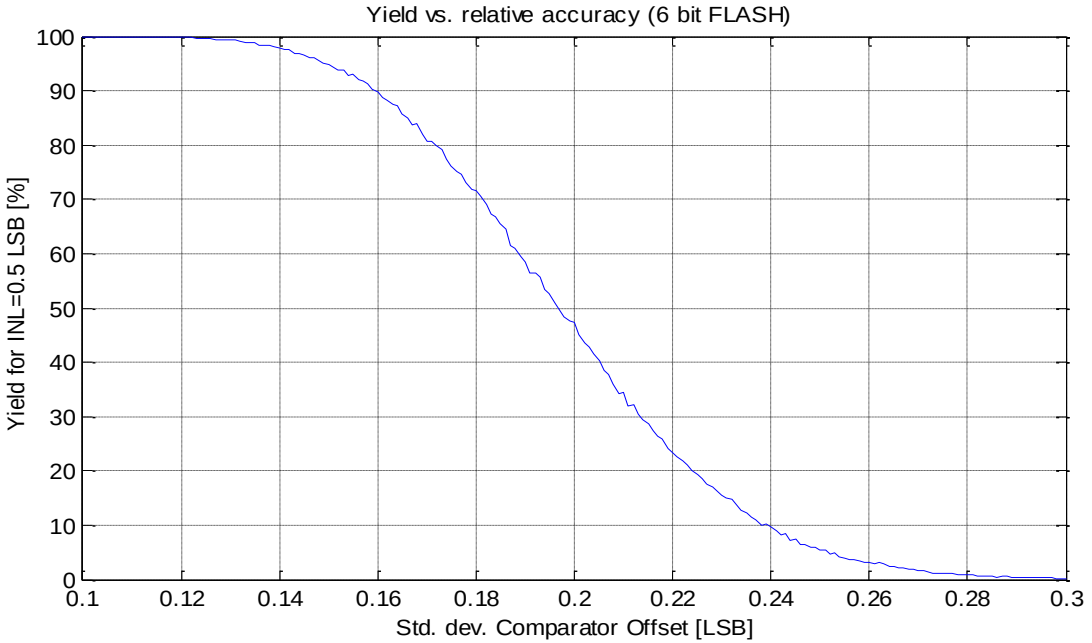
$$H(s) = \frac{\frac{gm1}{C2.CT^2}\cdot\left(gm3.gm9 - C2.Cc.s^2\right)}{s^3 + \frac{gm3.(CL+Cc) - \beta.gm1.Cc}{CT^2}\cdot s^2 + \frac{gm3.gm9.Cc}{C2.CT^2}\cdot s + \frac{\beta.gm1.gm3.gm9}{C2.CT^2}}$$

$$Vnamp = \sqrt{\frac{2}{3}\frac{K\cdot T}{Cc}\cdot\frac{1+\frac{Vdsat1}{Vdsat7}}{f}}$$

$$CT = \sqrt{C1.CL + C1.Cc + CL.Cc}$$

Yield Simulation of a flash



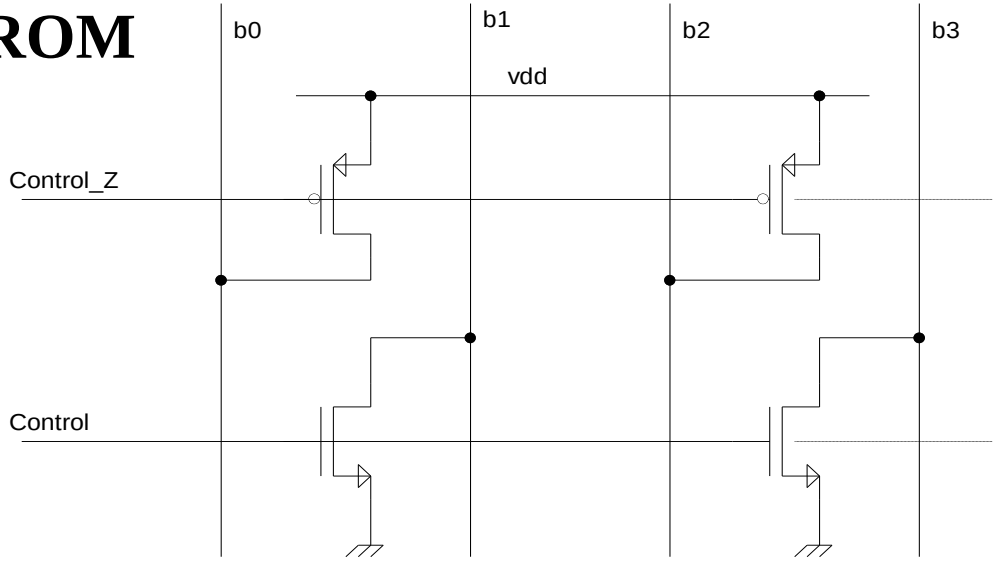


Yield of a 6 bit flash for INL=0.5LSB

$$\sigma^2(Vos) = \frac{A_{vt}^2}{(WL)_i} + \frac{(V_{GS} - V_T)^2}{4} \cdot \frac{A_\beta^2}{(WL)_i} \approx \frac{A_{vt}^2}{(WL)_i}$$

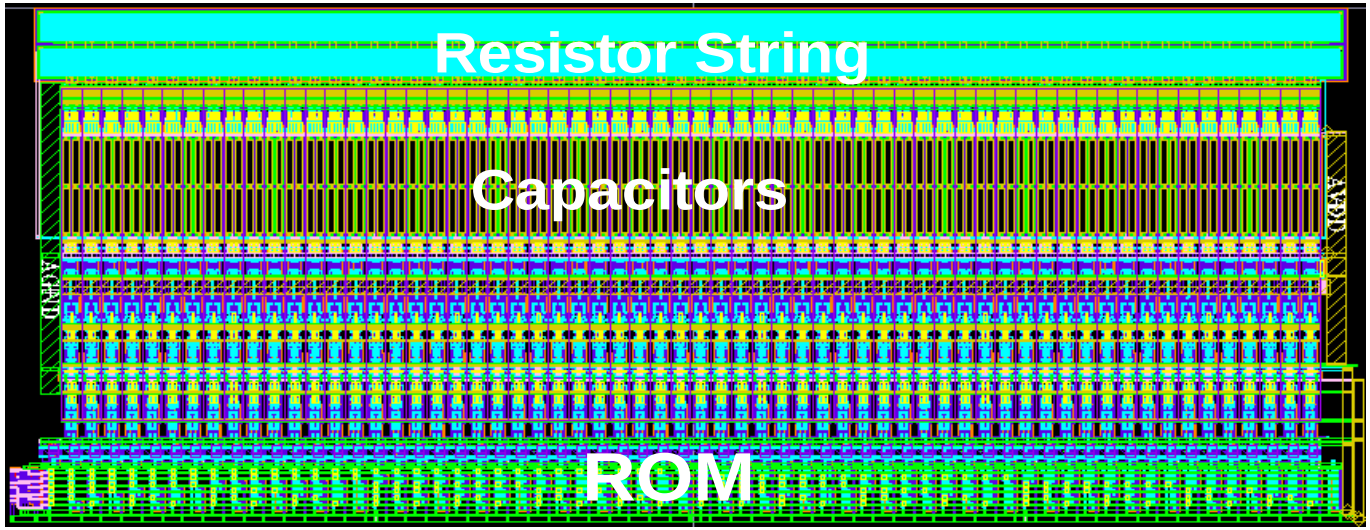
ROM Implementation

ROM



Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

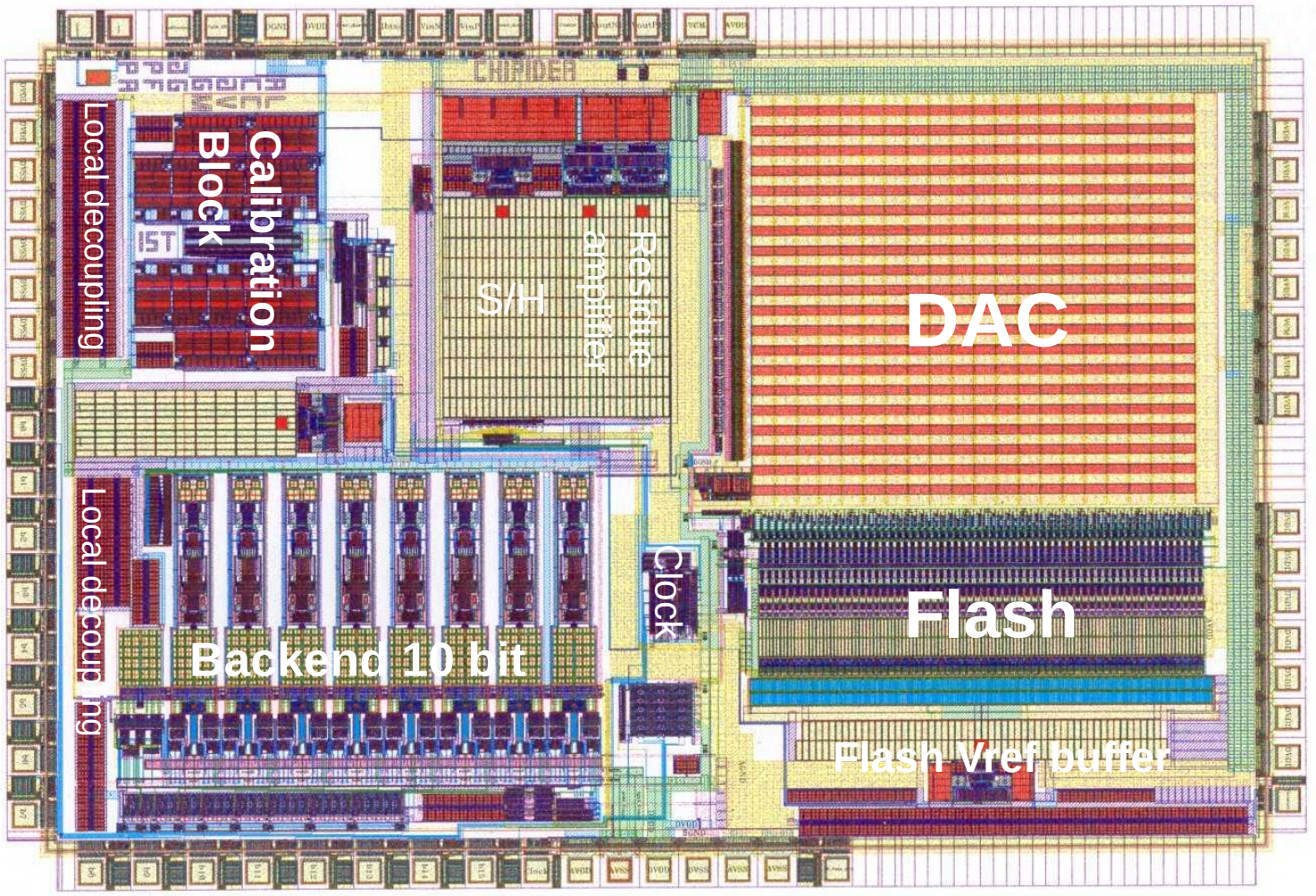
Figure 29.1 Comparison of digital input codes.



Area = 1.7 * 0.72 mm^2

Comparator

15-bit 10MS/s pipeline ADC Chip Layout

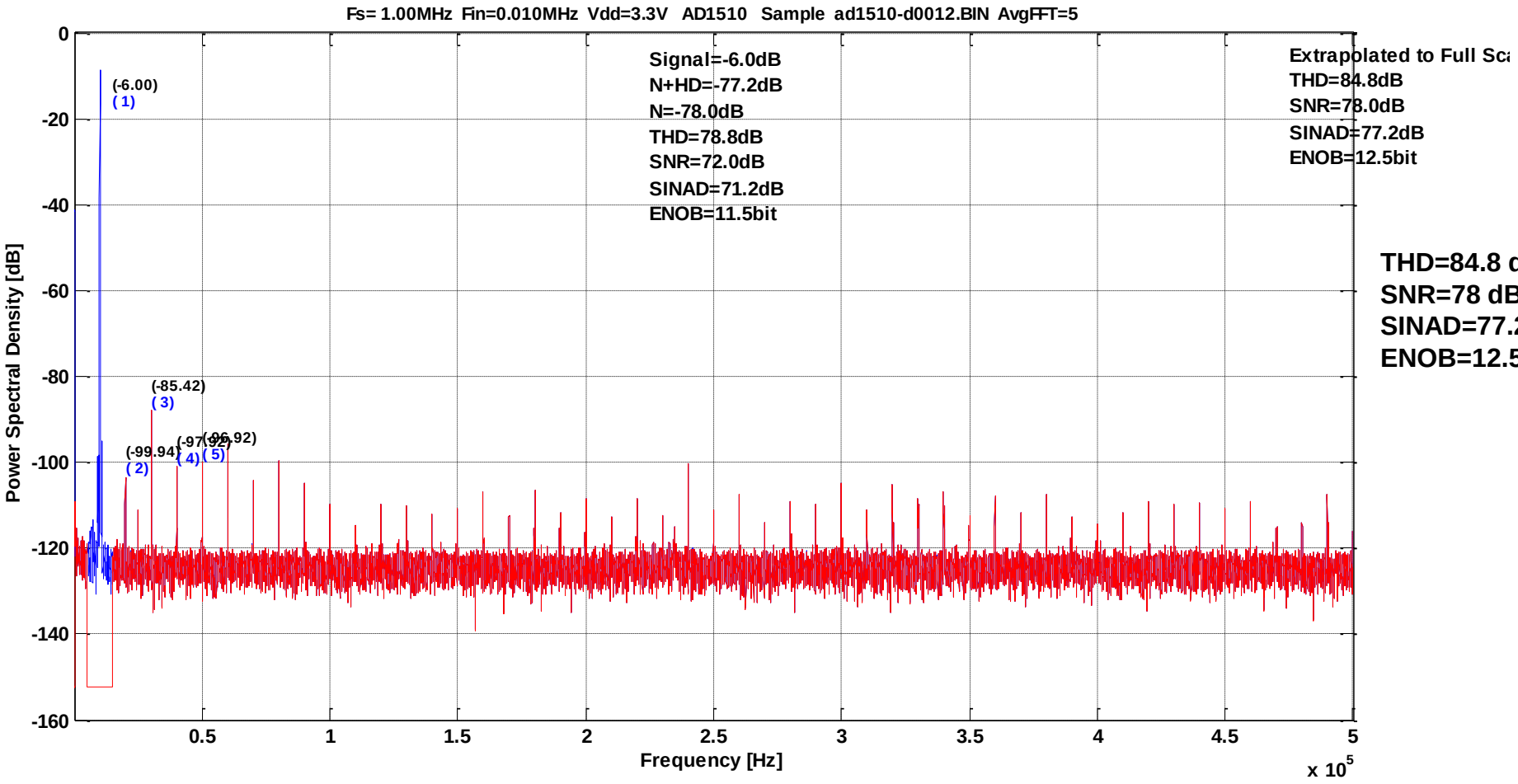


Summary

Resolution	15 bit
Conversion rate	10 Ms/s
Power consumption	320 mW
Power supply	2.7-3.3V
Input range	1.1V
SNDR	77.2 dB
THD	84.8 dB
ENB	12.5 bit
DNL, *fin* = 9.5 kHz	1.5 LSB at 15-bit
INL, *fin* = 9.5 kHz	3.3 LSB at 15-bit
Chip area	3.23 mm*4.75 mm
Core area	2.8 mm * 4.3 mm
Process technology	0.35 μm CMOS single poly 5-metal

Evaluation of the linear pipeline ADC

Full Converter Experimental Results

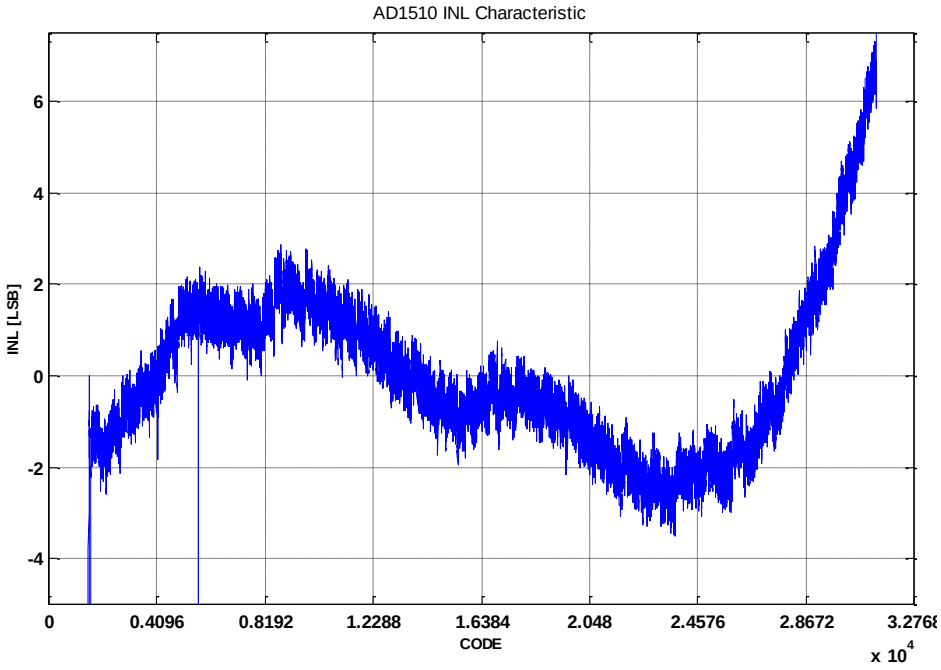


THD=84.8 dB
SNR=78 dB
SINAD=77.2 dB
ENOB=12.5 bit

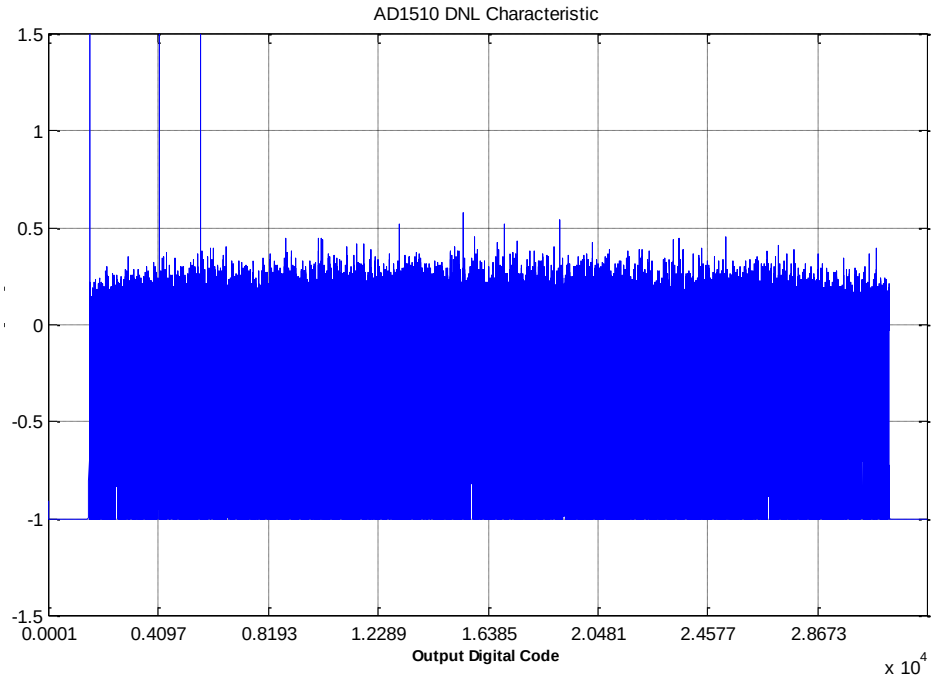
Evaluation of the linear pipeline ADC

Full Converter Experimental Results

Measured INL



Measured DNL

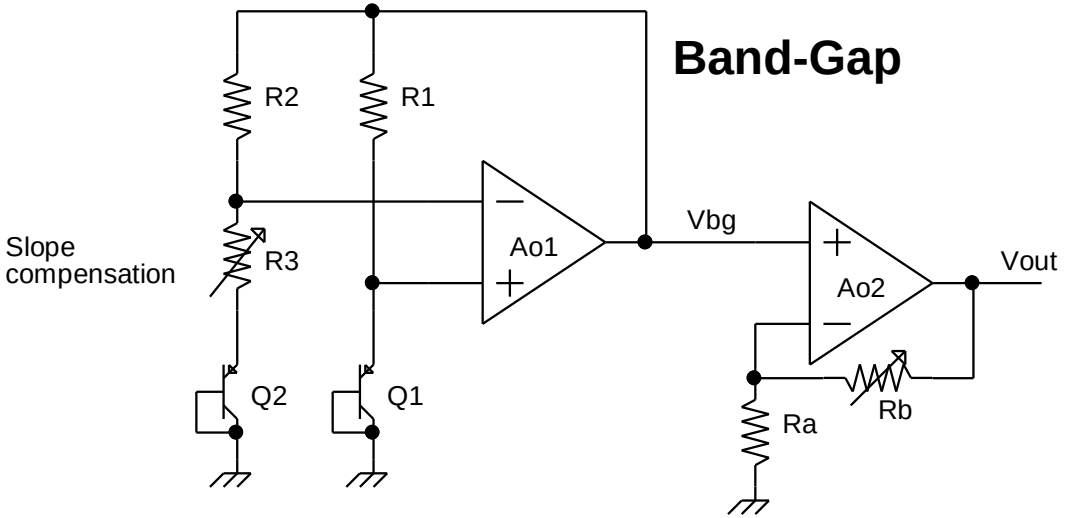


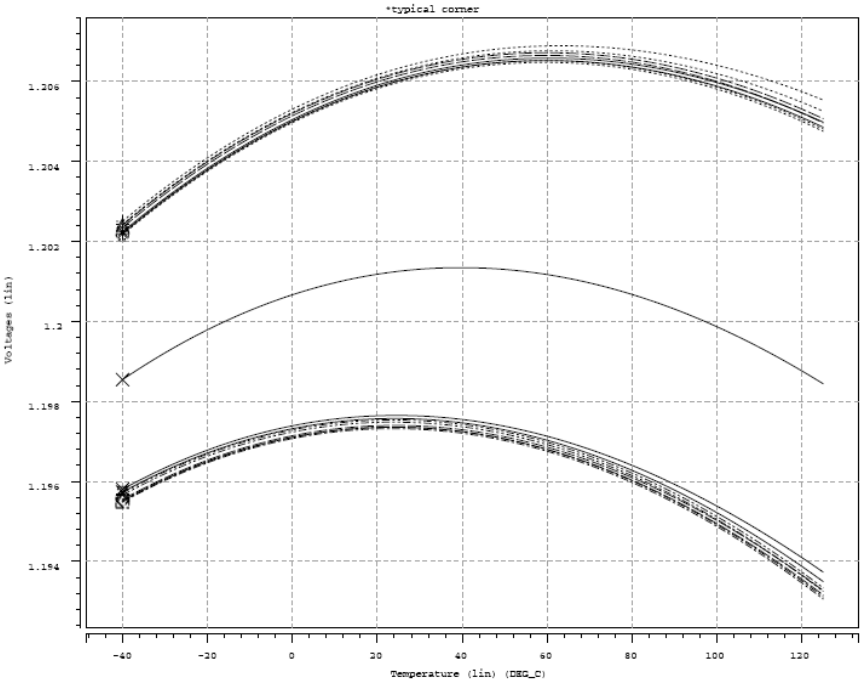
Vdd=3.3V
Fs=1MHz
Fin=9.5kHz
Vin=1.1V

16 million samples

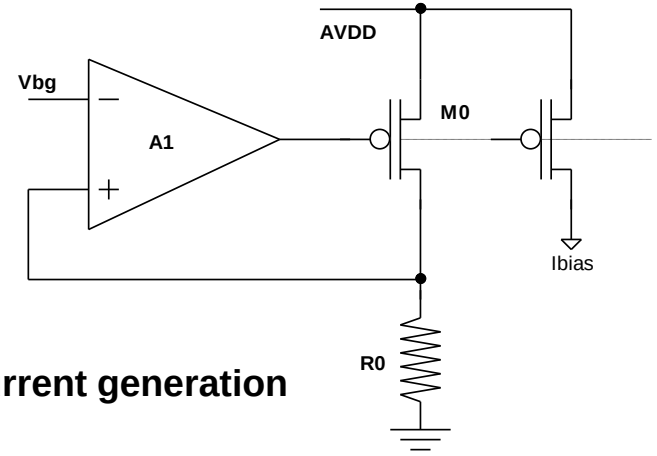
Auxiliary Blocks

Band-Gap

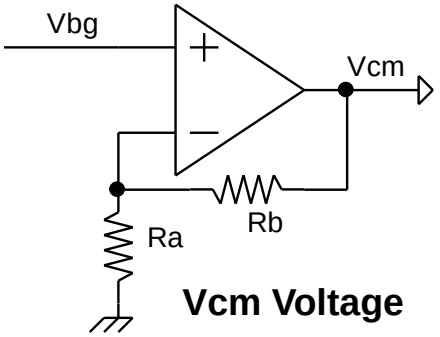




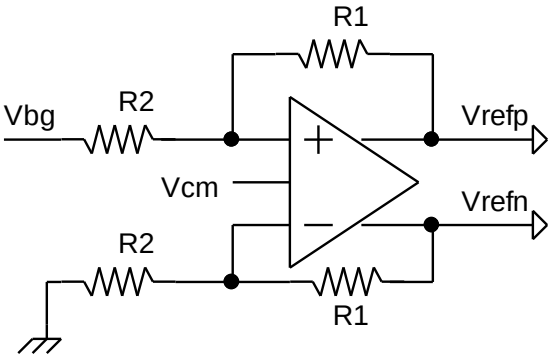
$$V_{OUT} = Vbe_1 - \left(1+\frac{R_2}{R_3}\right)V_{OS} + \frac{R_2}{R_3}V_T \ln\left(n\left(1-\frac{V_{OS}}{I_{R2}R_2}\right)\right)$$



Bias current generation

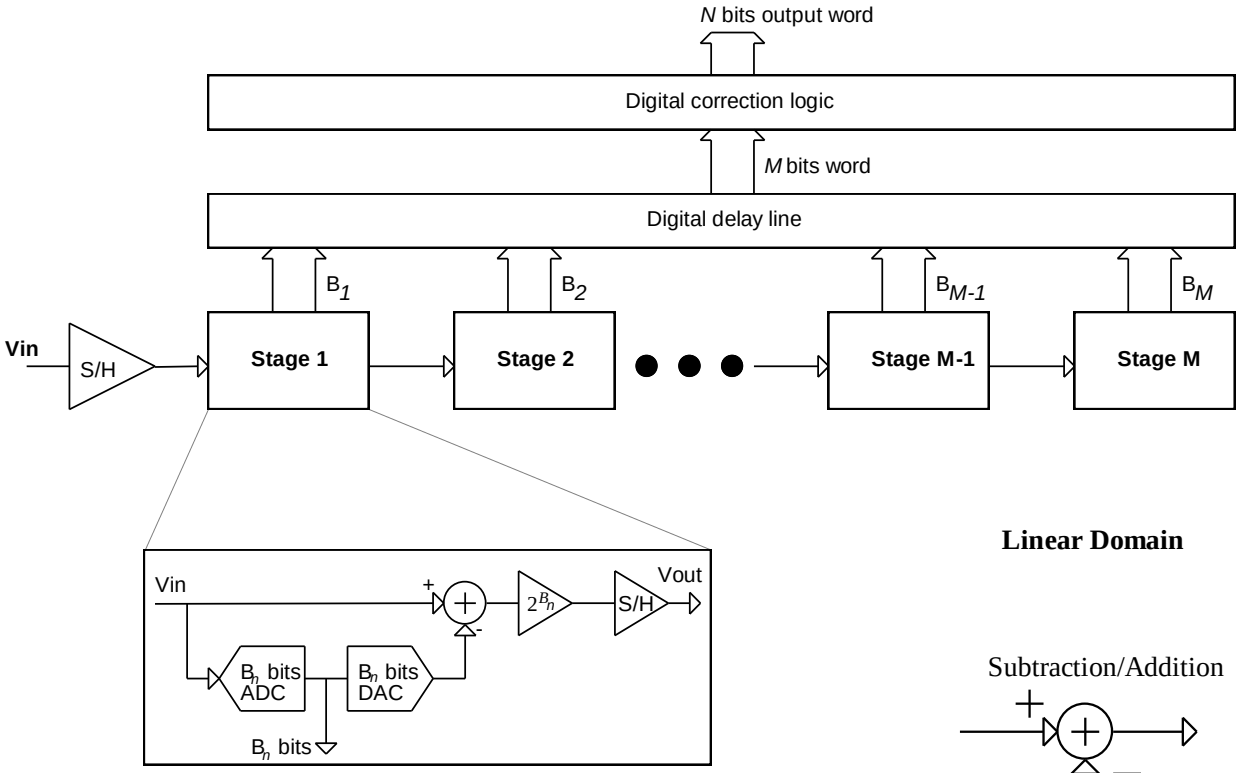


Vcm Voltage

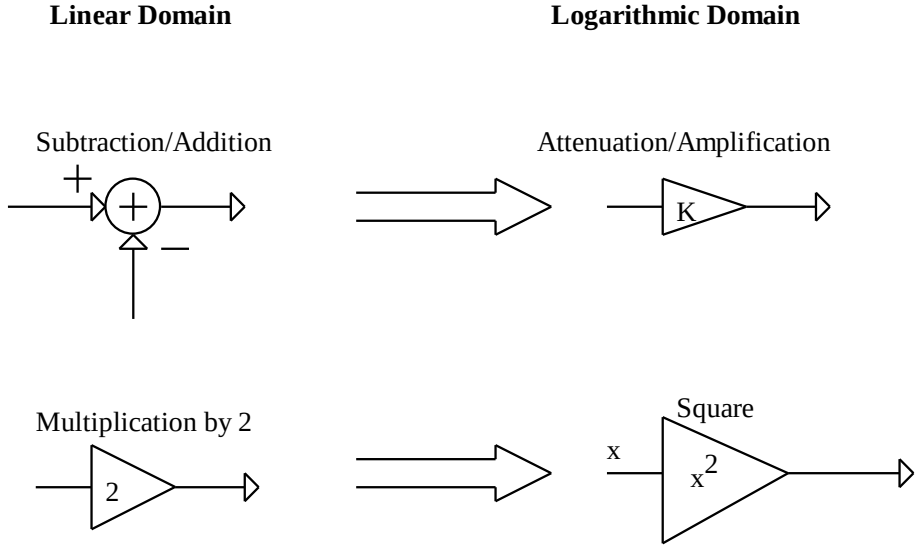


Reference Voltage

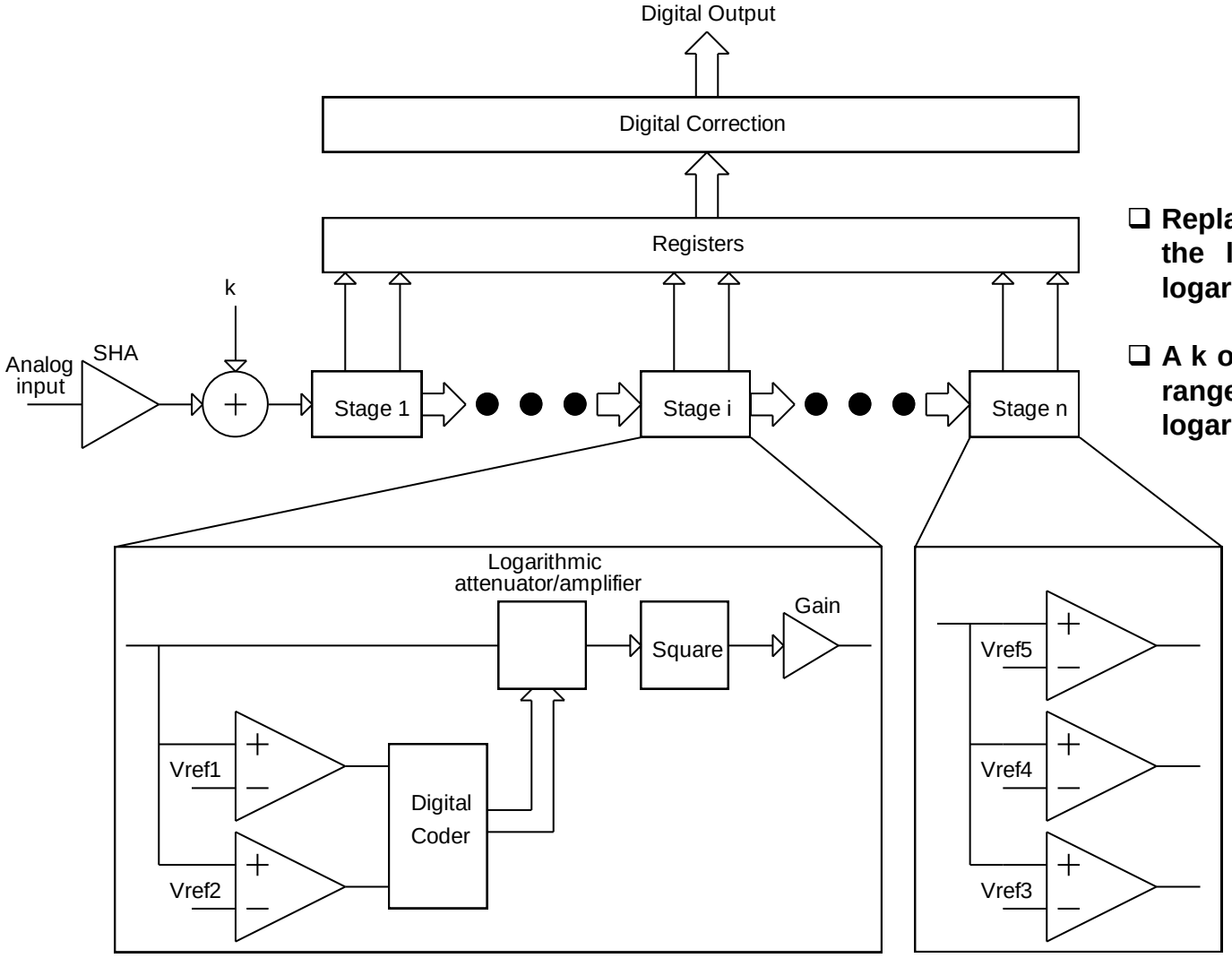
Classical Linear Pipeline Converter



- **The signal operations in the linear domain are replaced by their equivalent in the logarithmic domain**



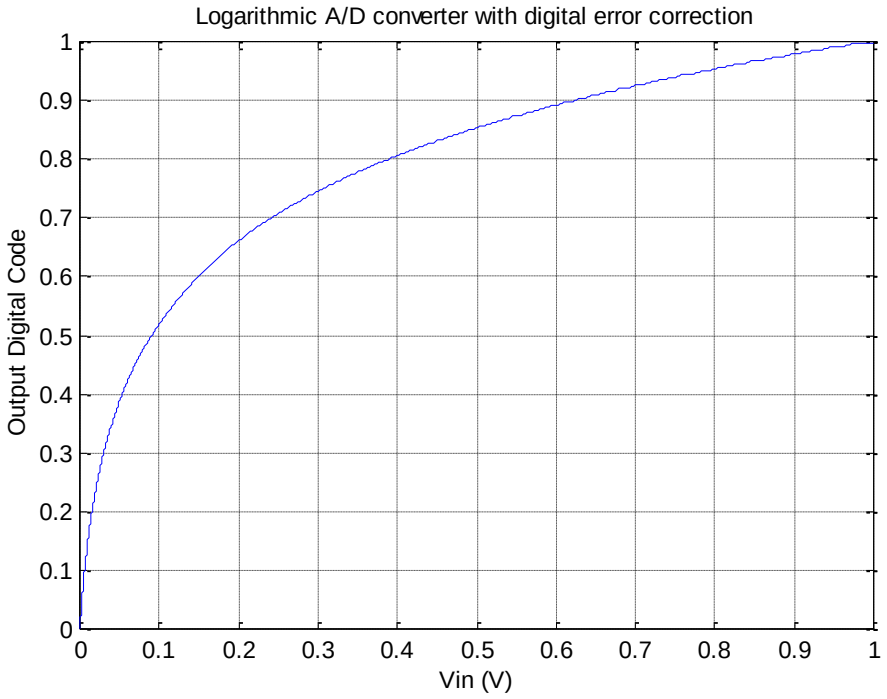
Logarithmic pipeline ADC architecture



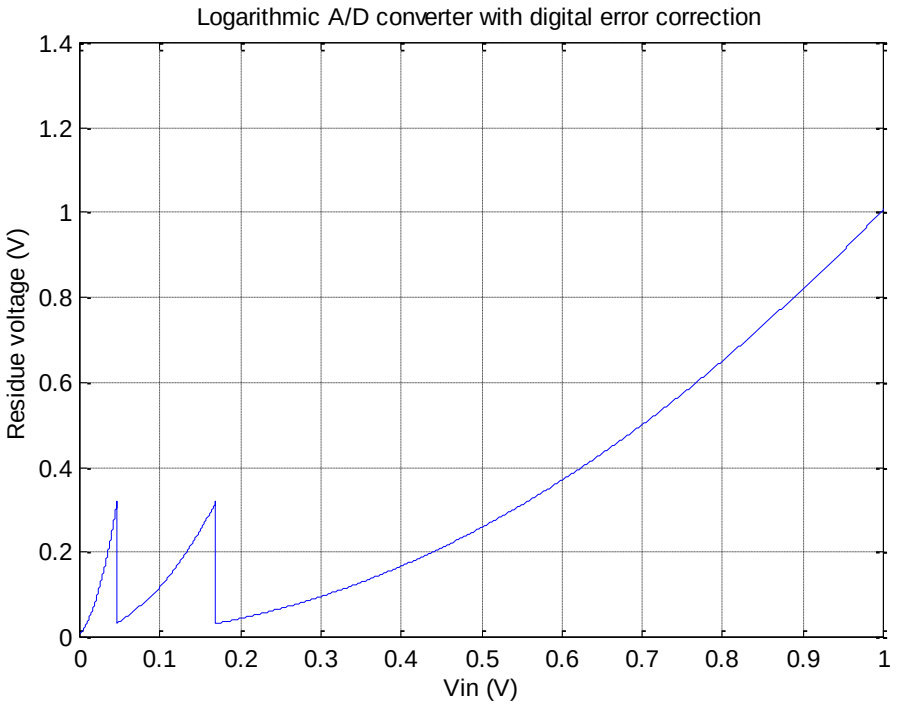
- **Replacing the signal operations in the linear pipeline we obtain a logarithmic pipeline ADC.**
- **A k offset at the input extends the range down to zero due to the logarithmic characteristic.**

Logarithmic pipeline ADC

Converter characteristic



Residue of first stage



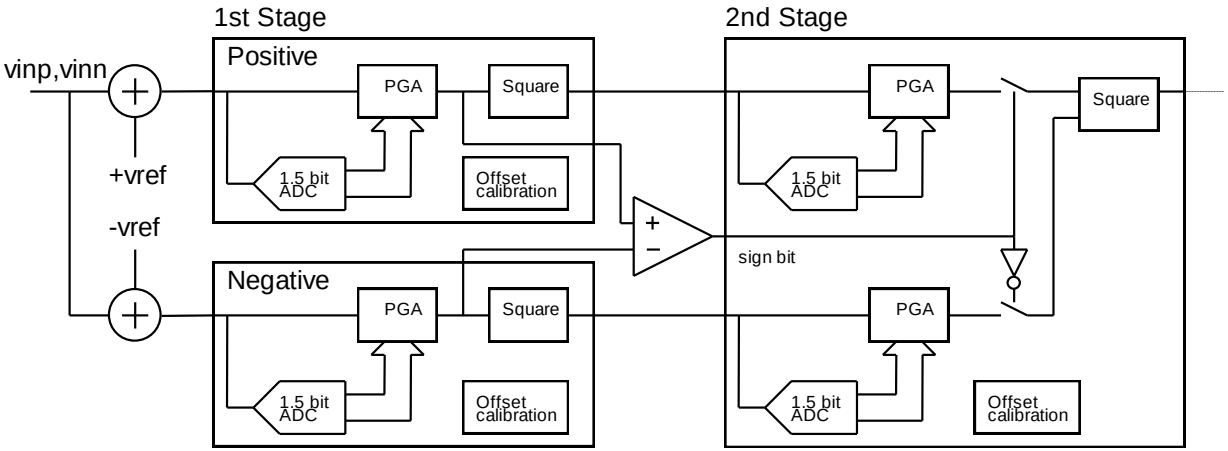
- Converter characteristics for positive input signals.
- The squarer gives a parabolic characteristic to the residue

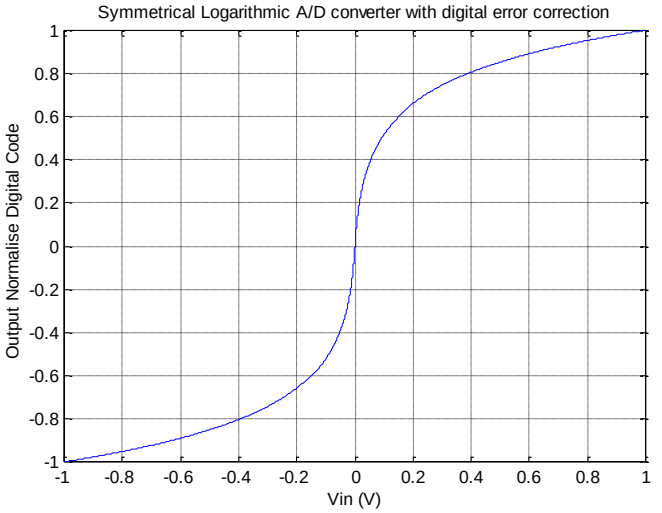
$$DR_{dB} = 20 \cdot \log_{10} \frac{1}{K \cdot \left(\left(\frac{1}{K} + 1 \right)^{\frac{1}{2^N - 1}} - 1 \right)}$$

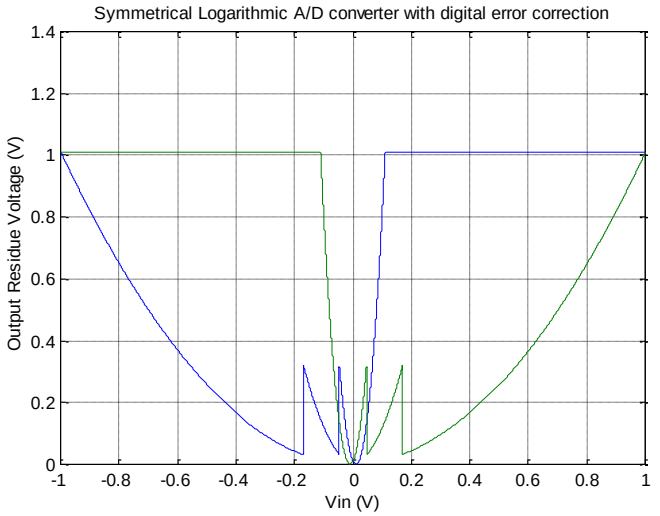
$$SNR_{dB} = 10 \cdot \log_{10} \frac{3 \cdot 2^{2N}}{\ln\left(1 + \frac{1}{k}\right)}$$

Logarithmic pipeline ADC

- Solution for bipolar characteristic



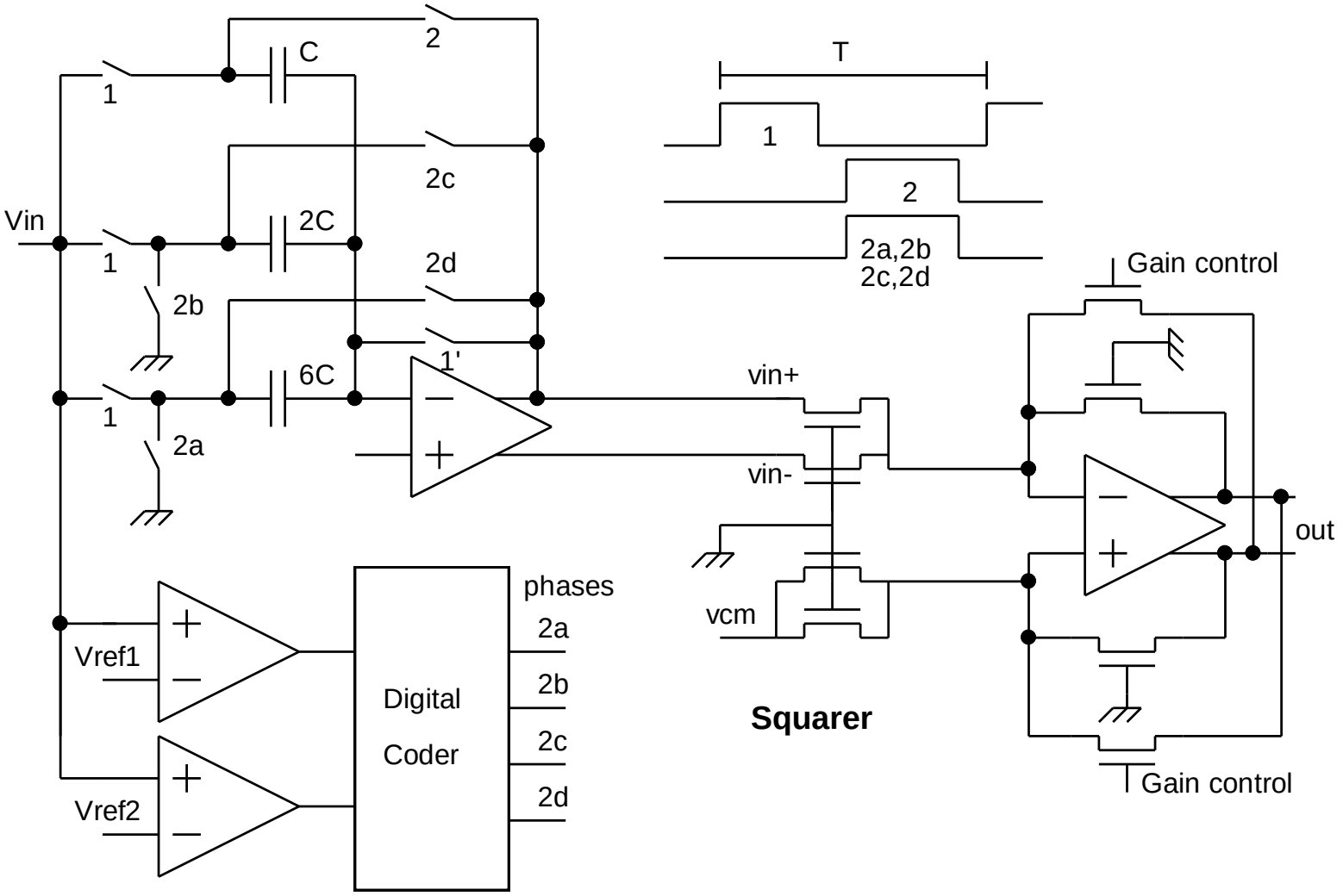




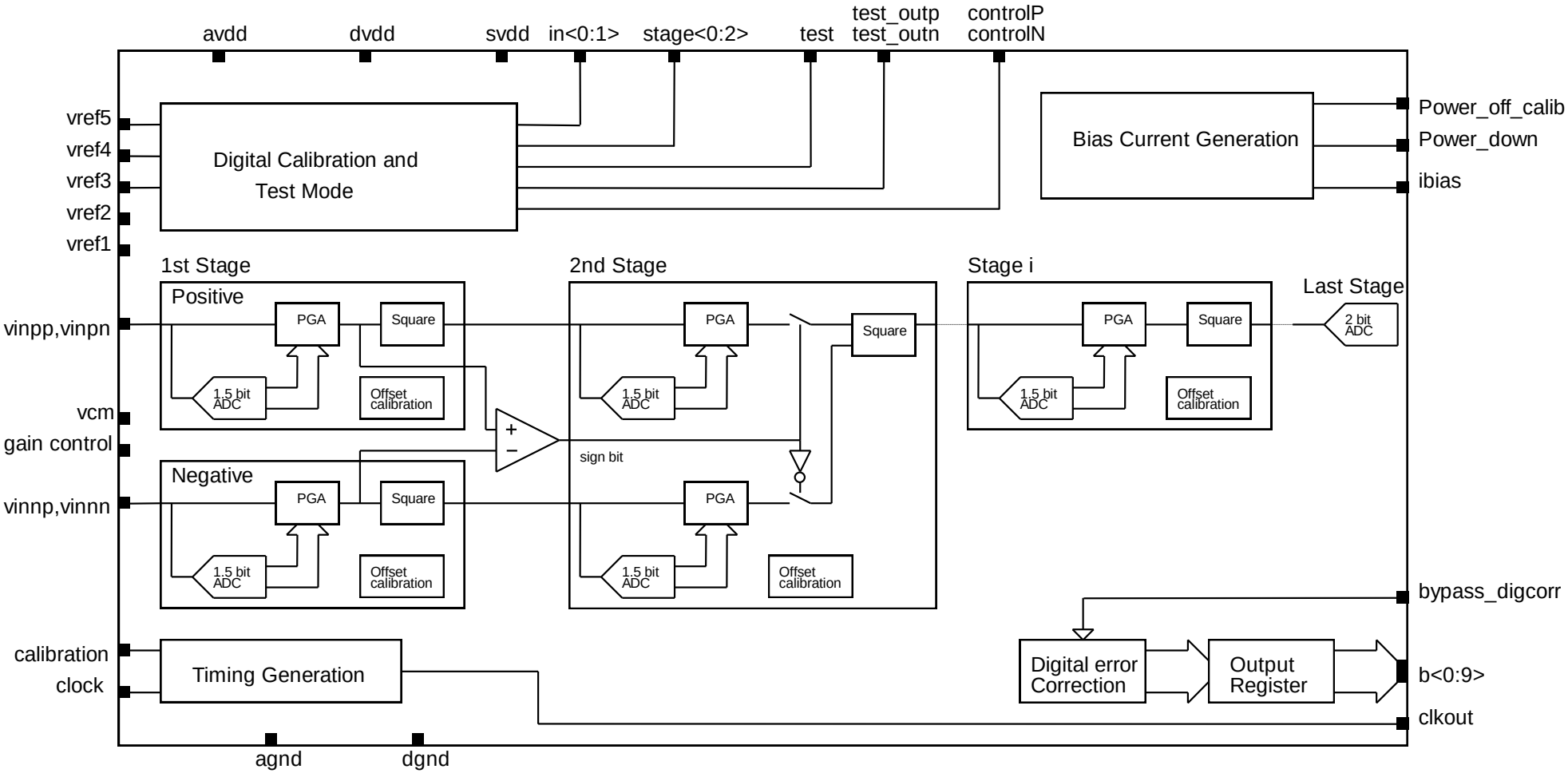
- **After first stage residue signal is always positive due to squarer.**
- **Following stages only process positive input signals.**
- **The sign bit is extracted by the intersection of the input stage characteristics.**
- **Second stage is split in two to allow the sign bit decision**

Logarithmic pipeline ADC

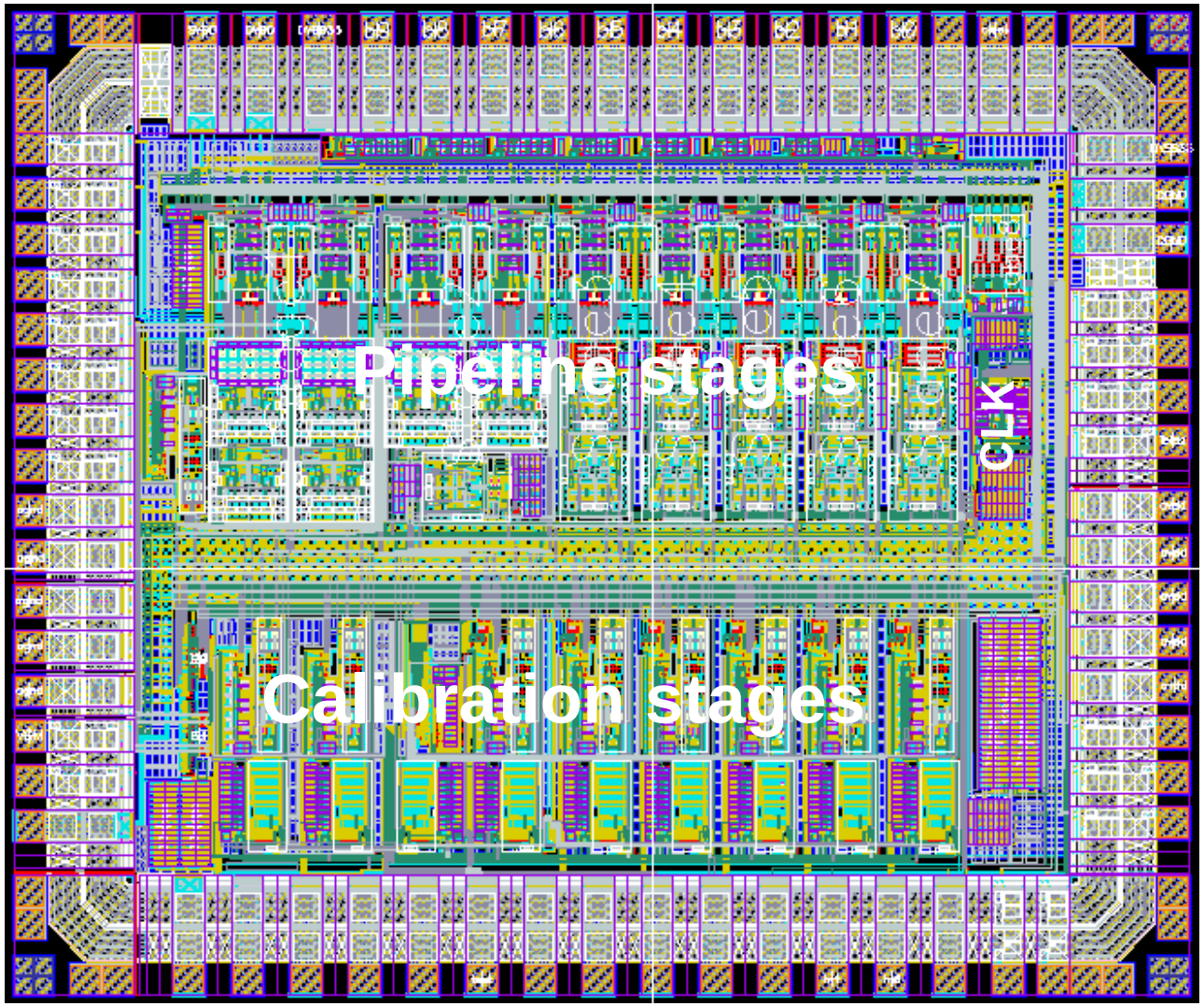
1.5-bit pipeline stage block diagram



Architecture of the 9-bit 10MS/s logarithmic pipeline ADC



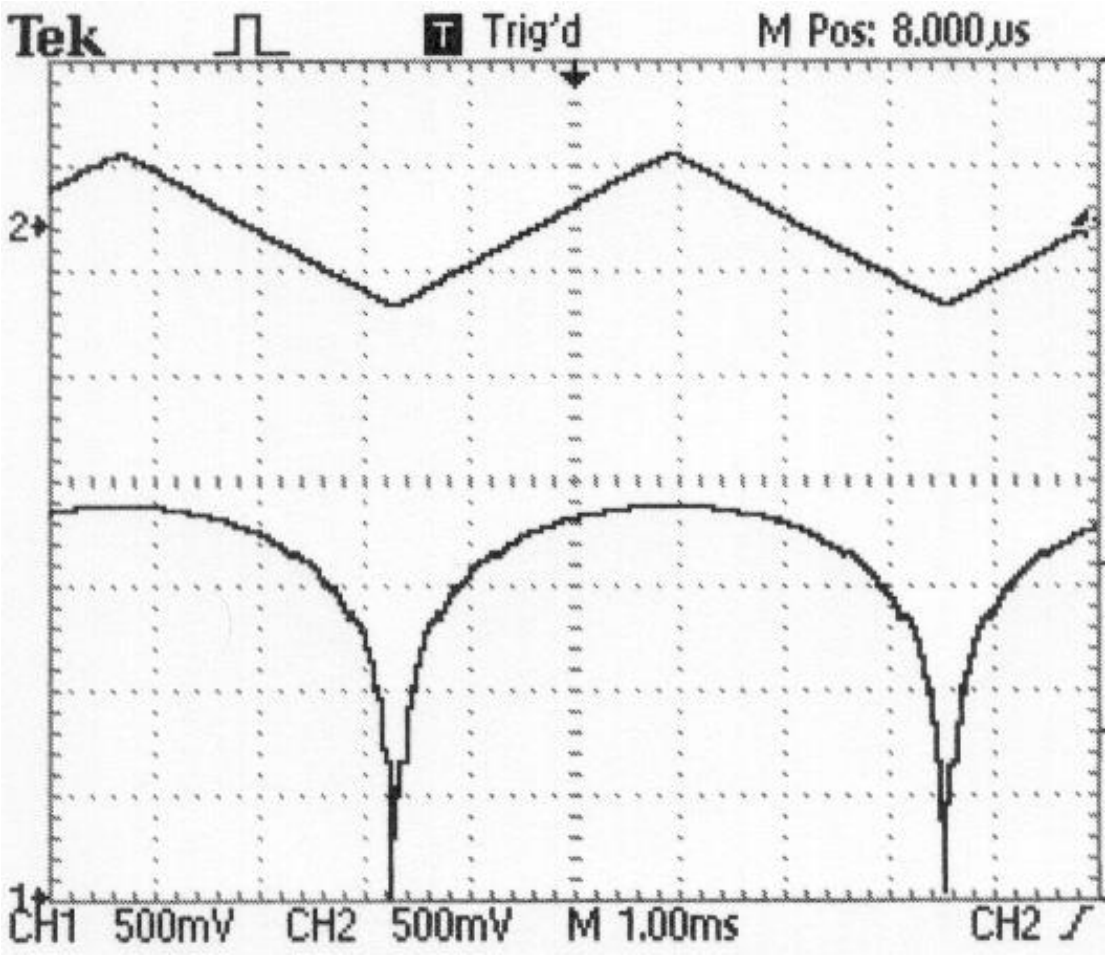
9-bit 10MS/s logarithmic pipeline ADC Chip Layout



Summary

Resolution	9 bit
Conversion rate	10 Ms/s
Power consumption	478 mW
Power supply	2.2-2.7V
Input range	1V
SNR	45.7 dB
Dynamic range	79.28 dB
Chip area	3.1 mm*2.6 mm
Process technology	0.25 μm CMOS single poly 5-metal

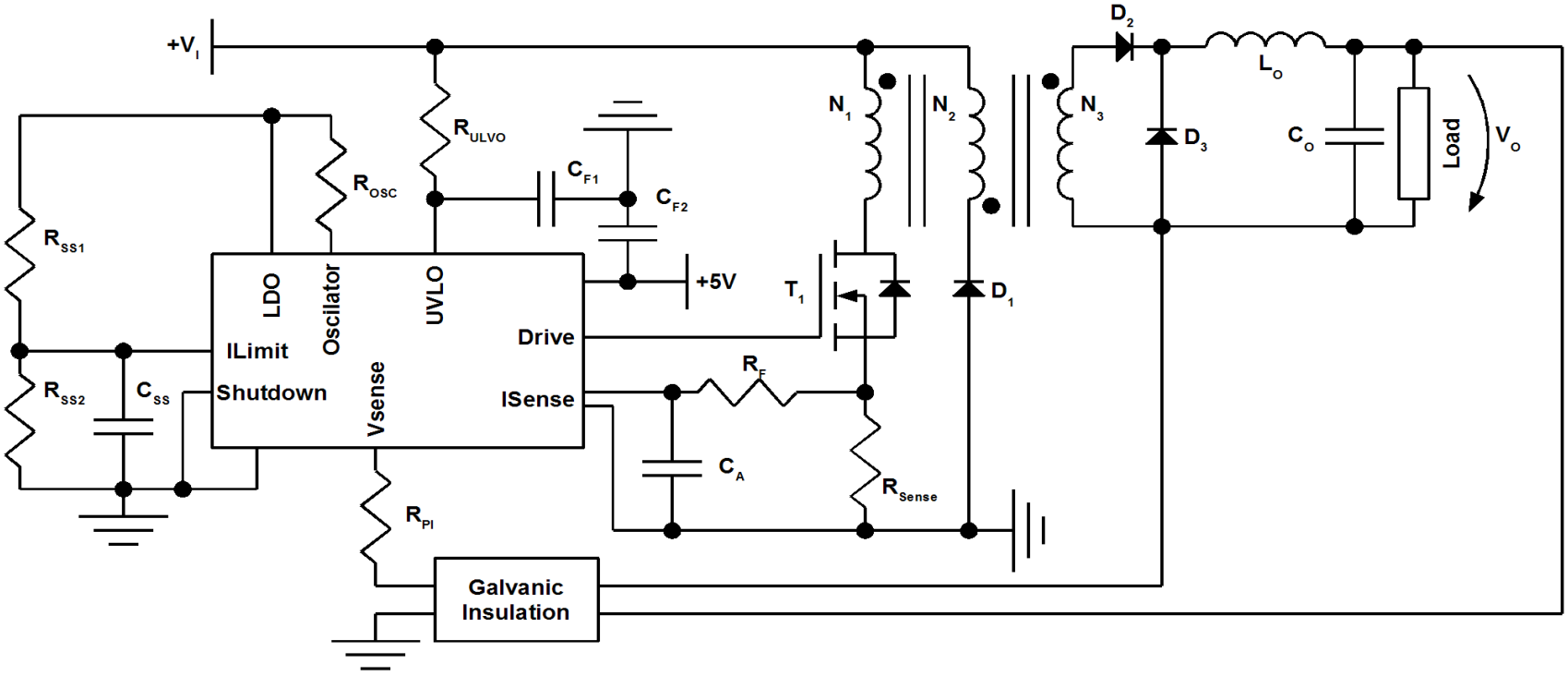
Evaluation of the logarithmic pipeline ADC



Measured output of the pipeline converter by injecting a triangular waveform of 250 Hz at the input, for a clock frequency of 1.3 MHz

Other Projects

DC-DC Controller for Space Application

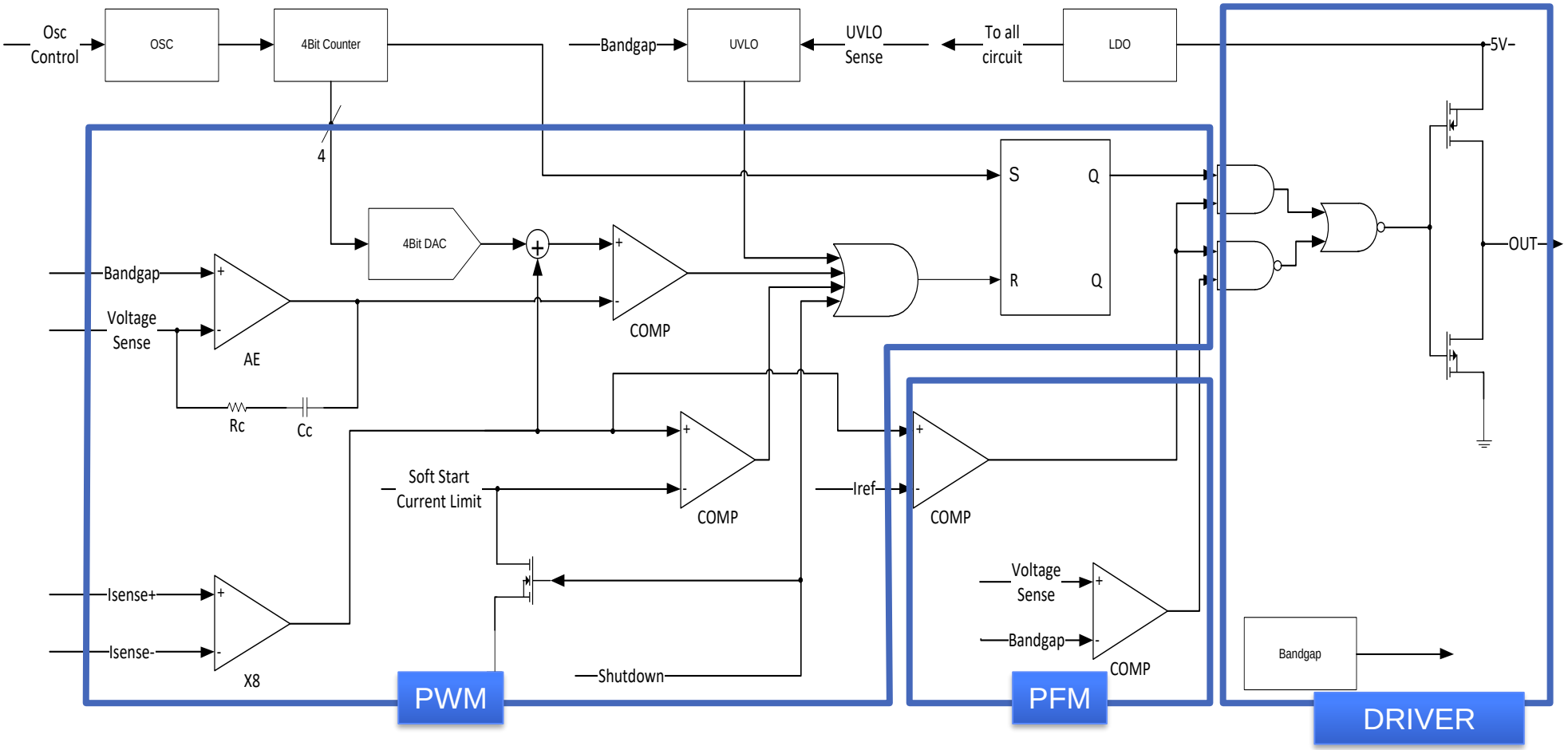


Radiation resistant isolated DC-DC converter using a forward topology

Controller Features

- Current mode control, cycle by cycle current limit
- Up to 2nF drive capability (to drive external power MOS)
- Soft-Start
- External shutdown/enable pin
- Adjustable oscillator frequency (up to 2MHz) using a single resistor
- PFM control mode for light loads to improve efficiency
- Radiation hardening
- Technology AMS 035 um CMOS

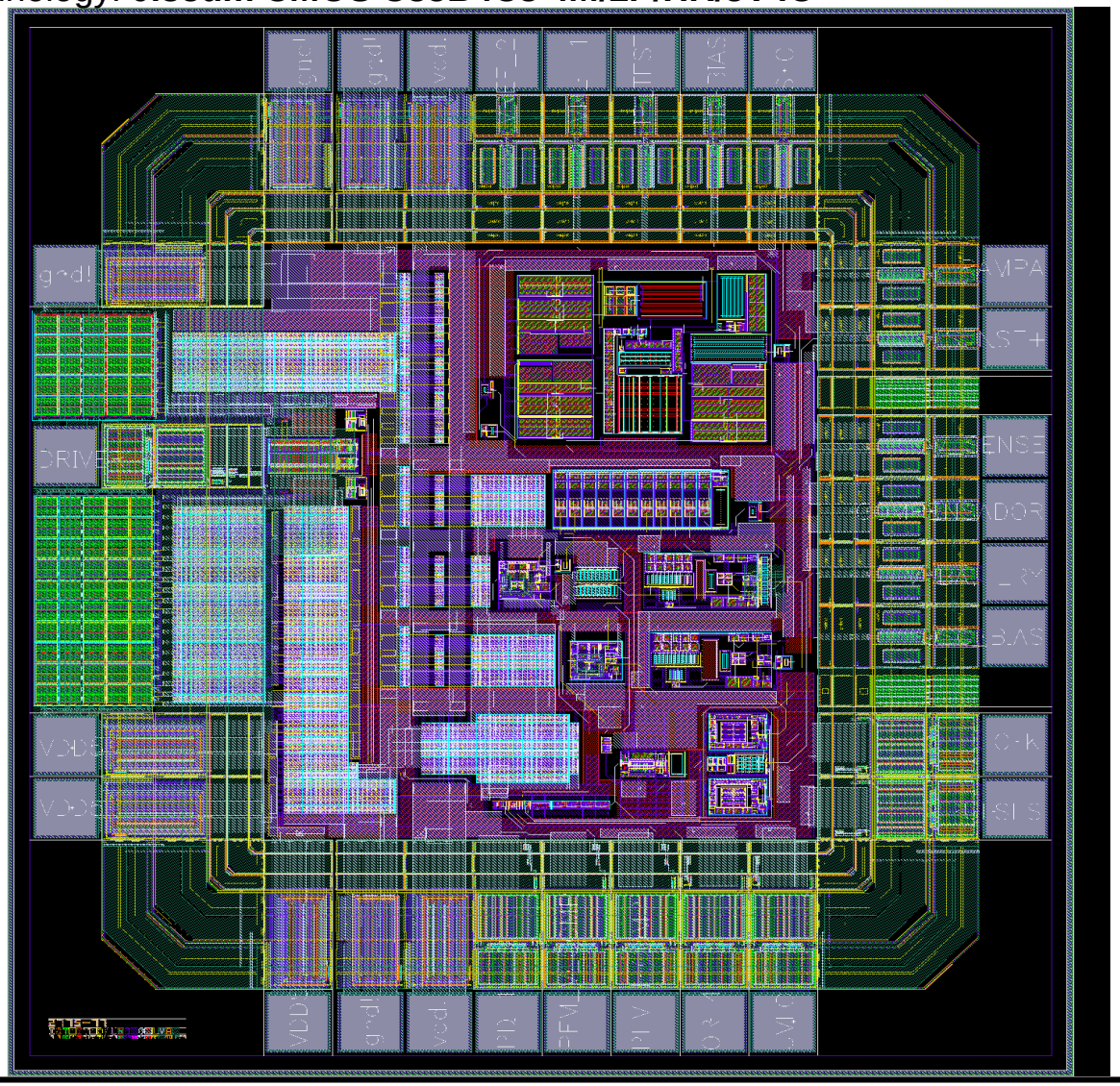
Controller:


Osc Control
OSC
4Bit Counter
Bandgap
UVLO
UVLO Sense
To all circuit
LDO
5V
4
4Bit DAC
S
Q
R
Q
OUT
Bandgap
Voltage Sense
AE
COMP
Rc
Cc
Soft Start Current Limit
COMP
Iref
COMP
Isense+
Isense-
X8
Shutdown
Voltage Sense
Bandgap
COMP
Bandgap
PWM
PFM
DRIVER

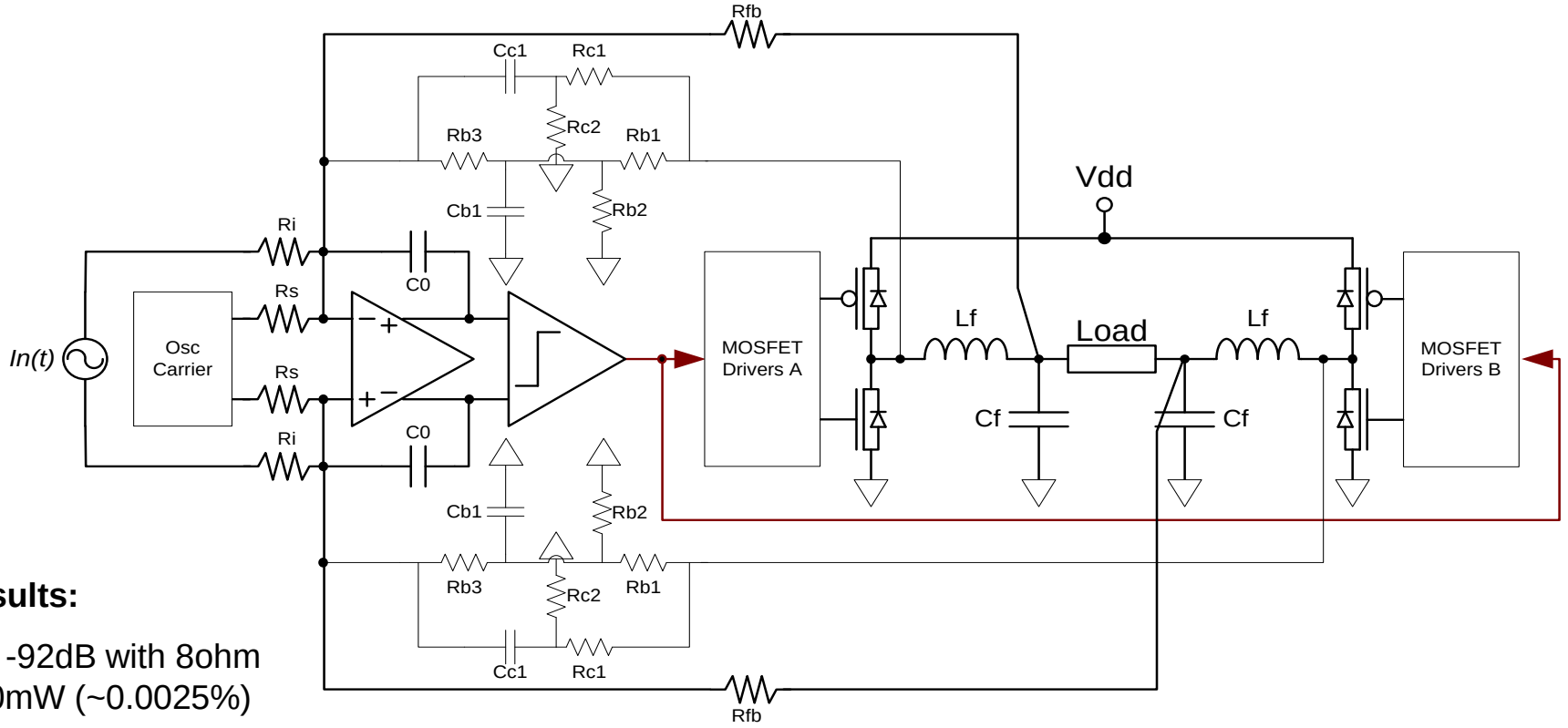
Integrated Prototype:

Area = 2.79 mm^2

Technology: **0.35um CMOS C35B4C3 4M/2P/HR/5V IO**



Class-D Audio Amplifier

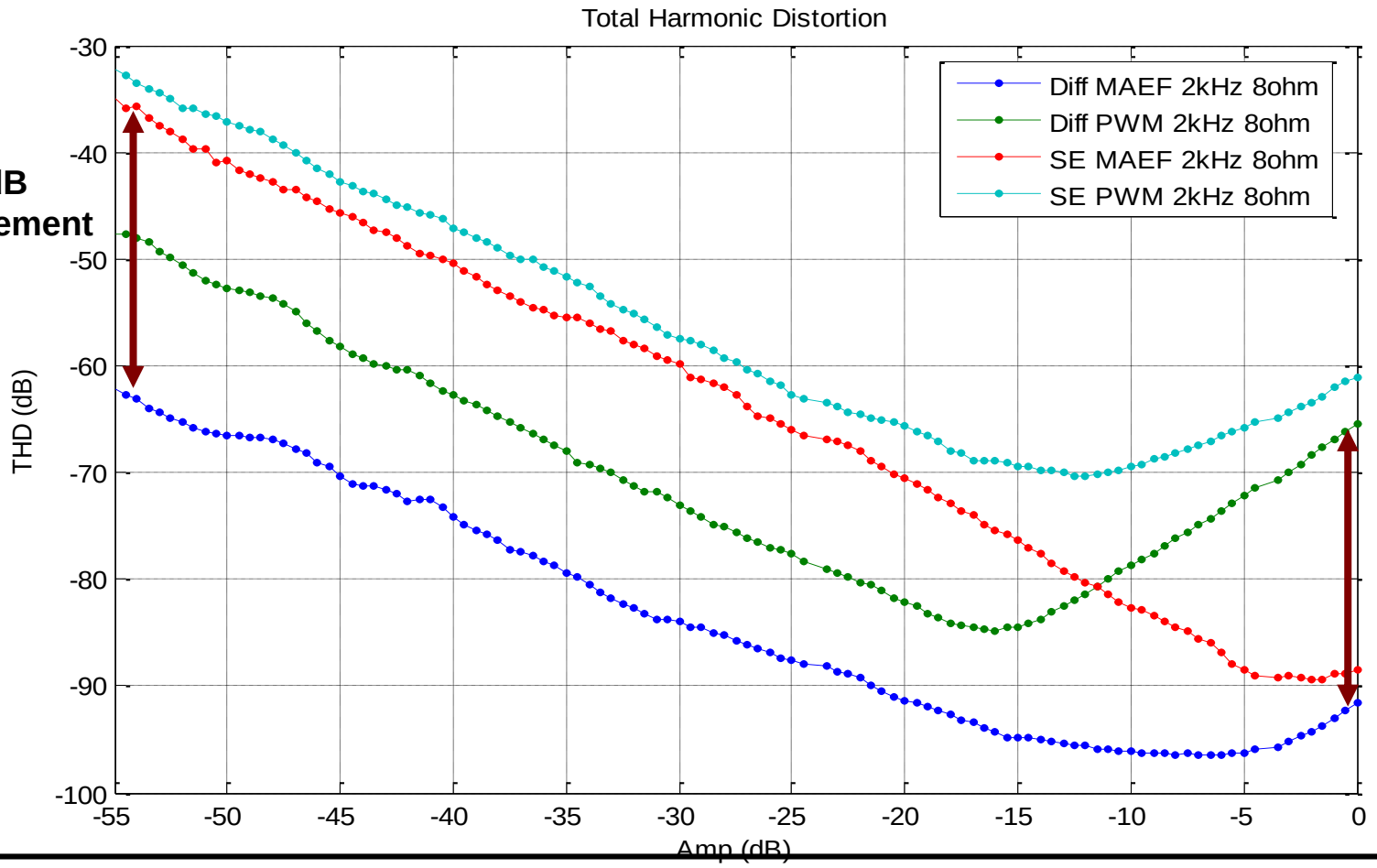


Results:

- THD below -92dB with 8ohm load at 680mW (~0.0025%)
- Over 26dB THD reduction when compared with open loop results
- *3.6μVrms closed-loop base-band noise*

Design Example – BTL Class-D

THD simulation results for Class-D with and without filter feedback – Comparison between BTL and SE Amp.



26dB improvement

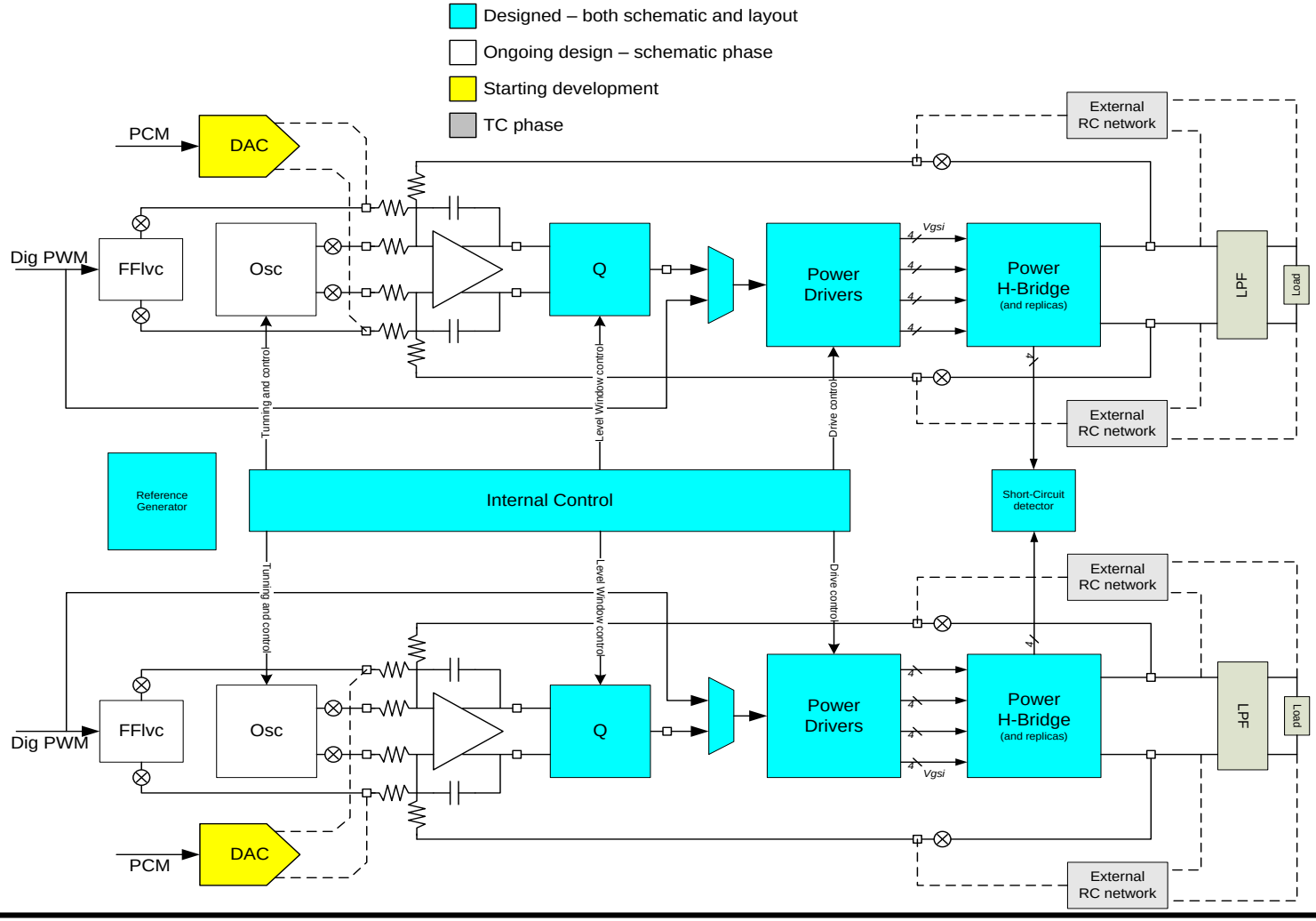
Two very long sweeps were conducted, each with 120 long transient simulations. The evolved filter improvement achieves over 26dB reduction for an 8 ohm load.

26dB improvement

The BTL Class-D exhibits lower intrinsic HD and higher open-loop diff gain, it has lower THD+N than the SE case.

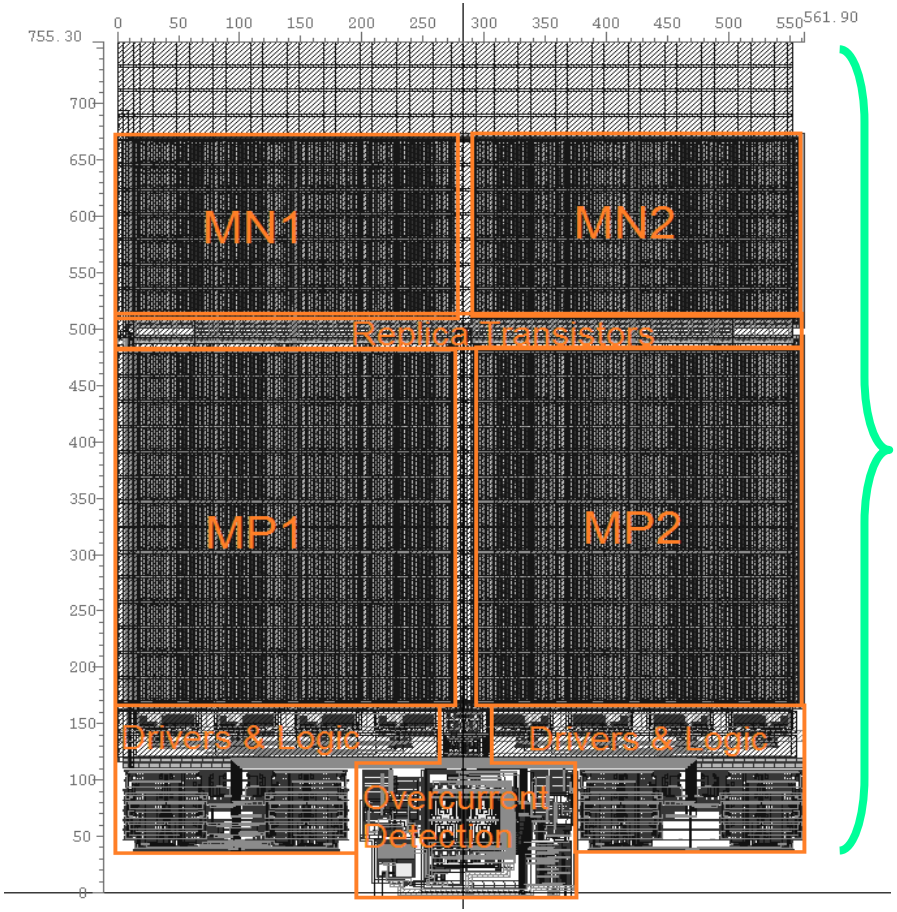
Test-Chip Architecture

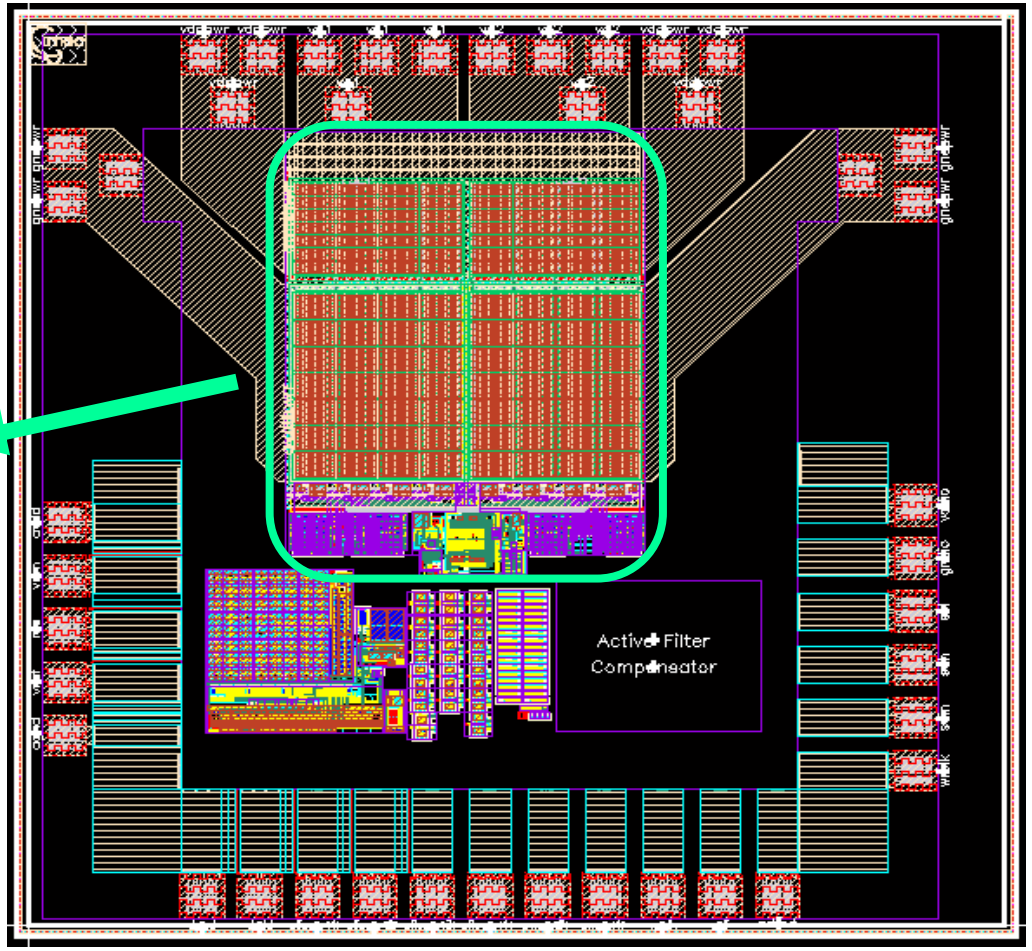
A Multi-mode Stereo Class-D Amplifier



Test-Chip Layout

Fully differential BLT Class-D Amplifier – Single Channel (UMC 018 um)





Note: MPW area constrains TC to single channel (1 reticule, 1.52x1.52 mm^2)

Summary

- A 15-bit 10MS/s pipeline ADC was presented
  - Linearity determined by matching accuracy of a current steering DAC.
  - A calibration scheme adjust the reference voltage of the backend pipeline, instead of calibrating the gain of the front-end stage.
- A 9-bit 10MS/s true logarithmic pipeline ADC derived from their linear counterparts.
  - Symmetrical characteristic with dynamic range independent of SNR
  - SNR of 44.3 dB for a dynamic range of 80 dB.
- Other Projects
  - DC-DC controller for Space Applications
  - Class D Audio Amplifier