ERC - Elementary Readout Cell

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18th April 2012

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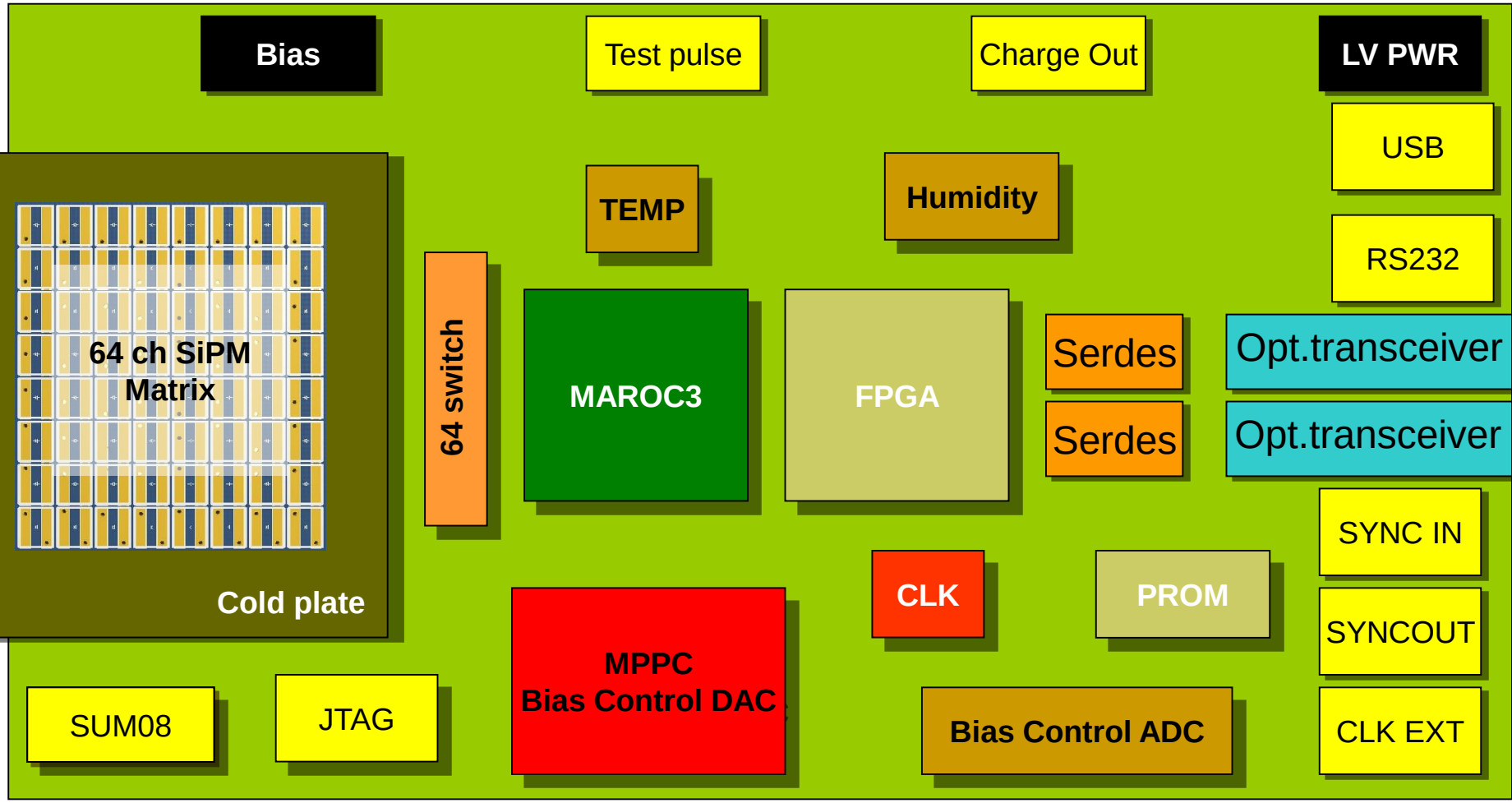
ERC Prototype Board

- MAROC3 chip (PQFP240 package)
- Altera Cyclone III (EP3C80F780C7N)

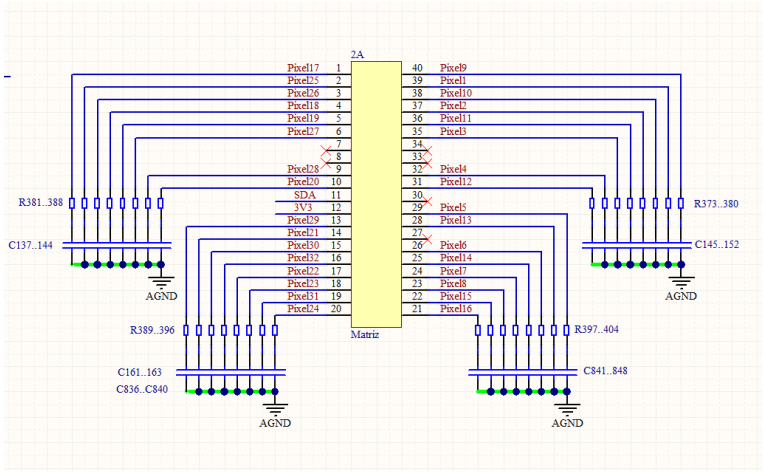
- LV regulation circuits (AVDD, VDD, VCIO, 3V3, 1V2,…)
- Bias supply regulation (DAC 14 Bits I2C)
- Bias supply monitoring (ADC I2C)
- 7 on-board sensors (TMP100 I2C)
- Internal CLK LVDS (125/60/40/80 MHZ)
- Humidity sensor (I2C)

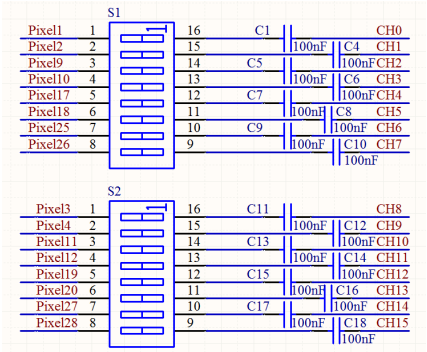
- USB link (FPGA DATA OUT)
- 2 SFP Optical Link (FPGA DATA OUT)
- External CLOCK connector
- External SYNC connector
- External NIM TRIGGER connector
- JTAG Connector
- External ASIC output monitoring connectors (charge, SUM08)
- Internal ASIC test pulse (common to 64 channels)

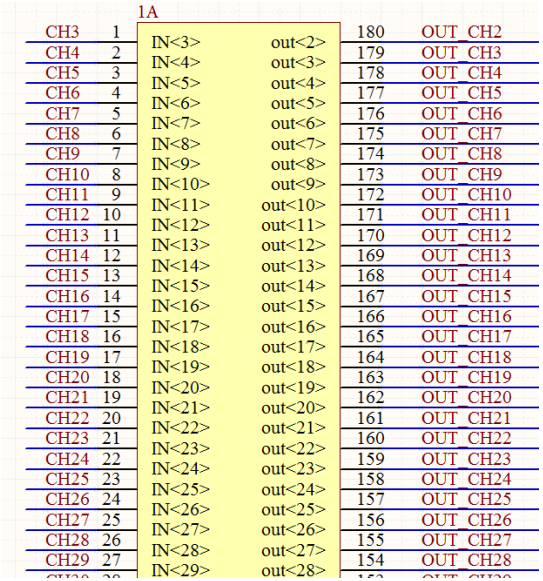
ERC Prototype Board

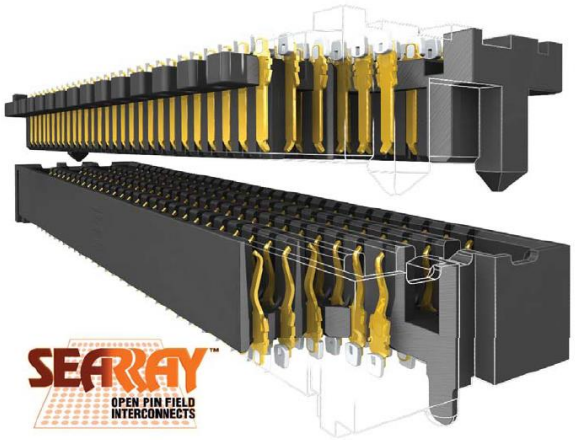


SiPM Analog Input with 50 ohm impedance control



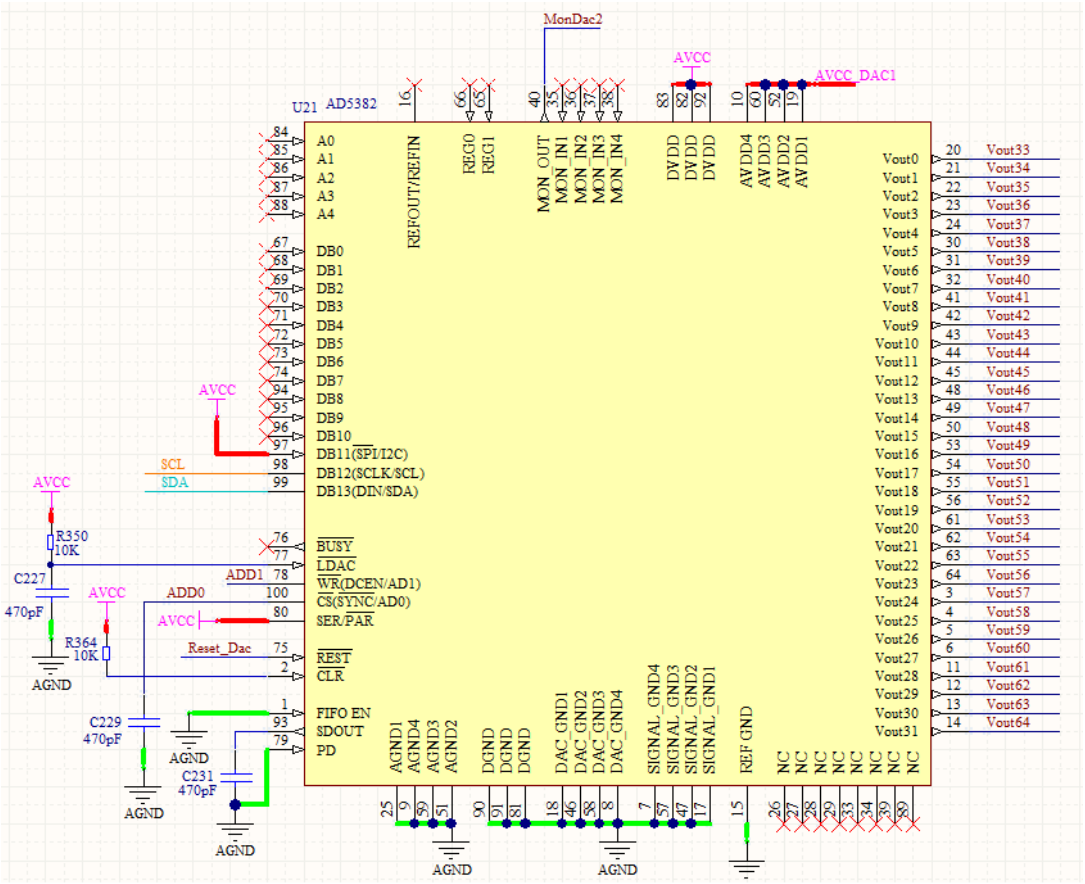


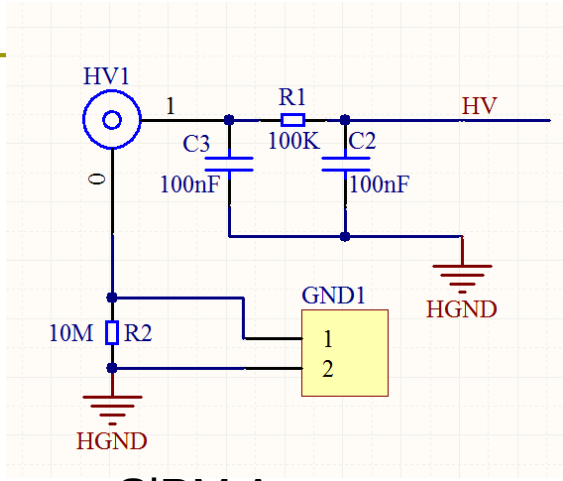




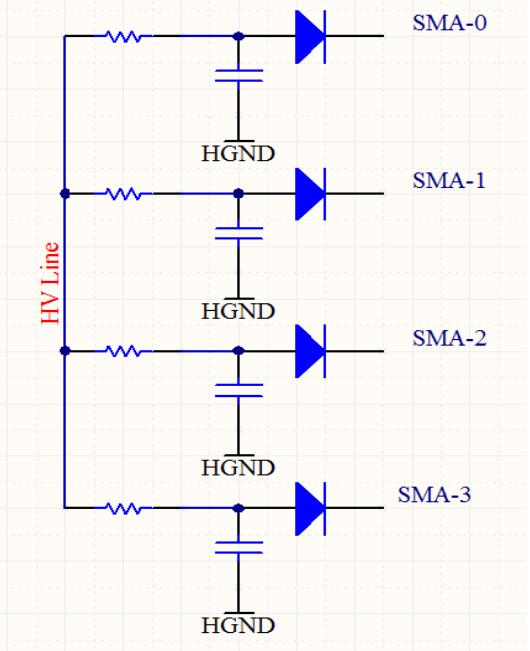
HV Regulation & Distribution

5 volts range with a 0.3mV LSB





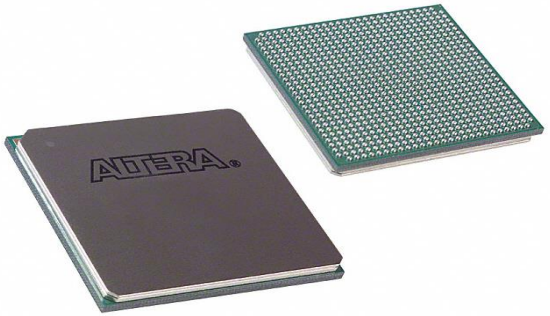
SiPM Array

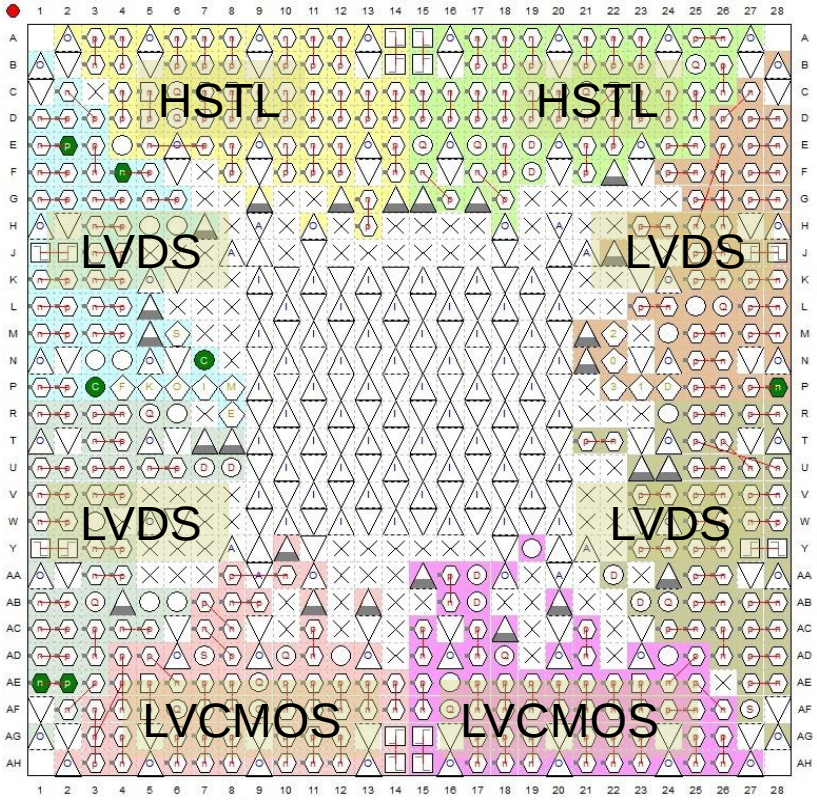


Cyclone III FPGA

Quantity	Item Number	Customer Reference	
	EP3C80F780C7N		Add to Order

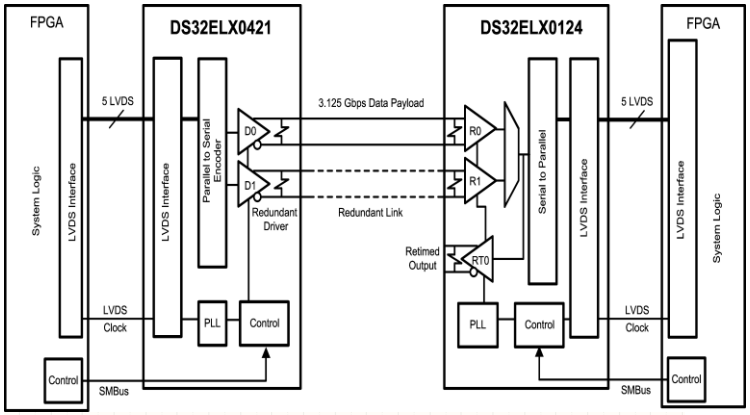
Datasheets	Cyclone III Brochure Cyclone III FPGA Family Errata Cyclone III Datasheet Cyclone III Design Guidelines Cyclone III Family Overview Cyclone III Device Handbook Vol2
Product Photos	780-FBGA Pkg
Standard Package	36
Category	Integrated Circuits (ICs)
Family	Embedded - FPGAs (Field Programmable Gate Array)
Series	Cyclone® III
Number of Logic Elements/Cells	81264
Number of LABs/CLBs	5079
Total RAM Bits	2810880
Number of I /O	429
Number of Gates	-
Voltage - Supply	1.15 V ~ 1.25 V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C
Package / Case	780-FBGA
Supplier Device Package	*
Other Names	544-2524
Lead Free Status	Lead free
RoHS Status	RoHS Compliant

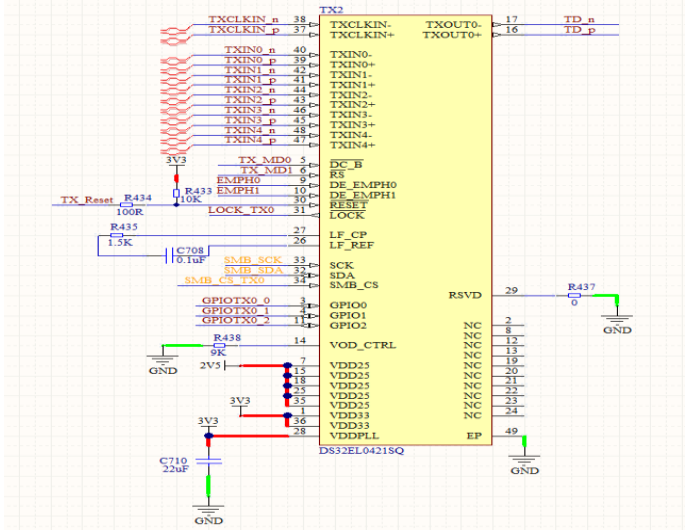


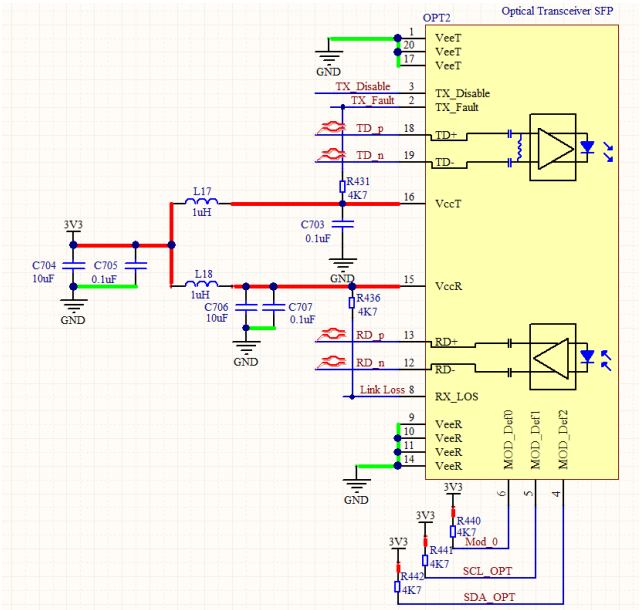


Optical Link up to 3.125Gbps

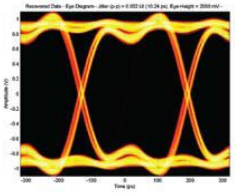
Transceiver from National Semicondutor





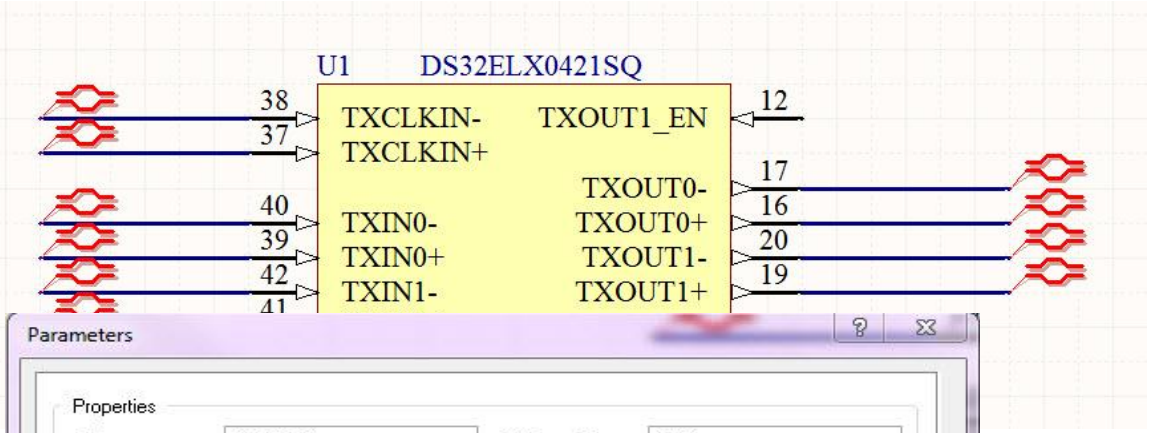


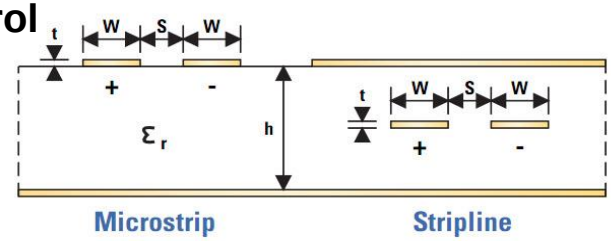
Digital Diagnostic SFP, 850 nm, 4.25/2.125/1.0625

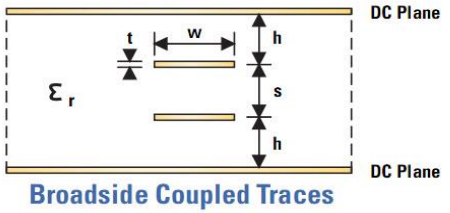


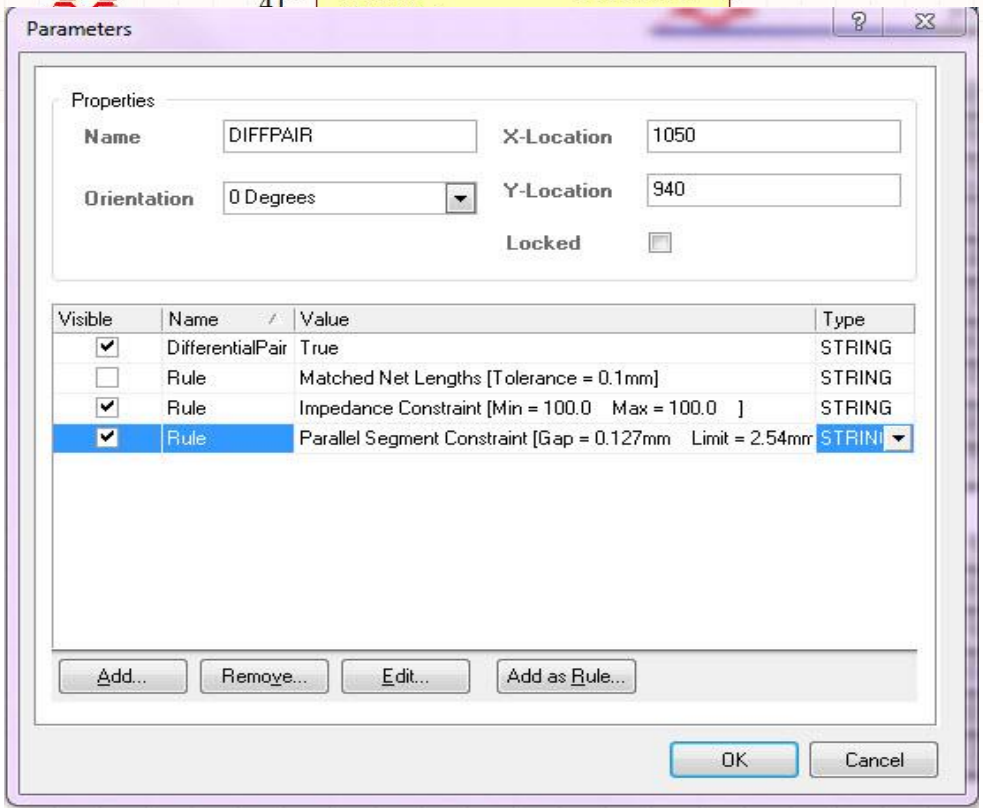
ERC Schematics Layout

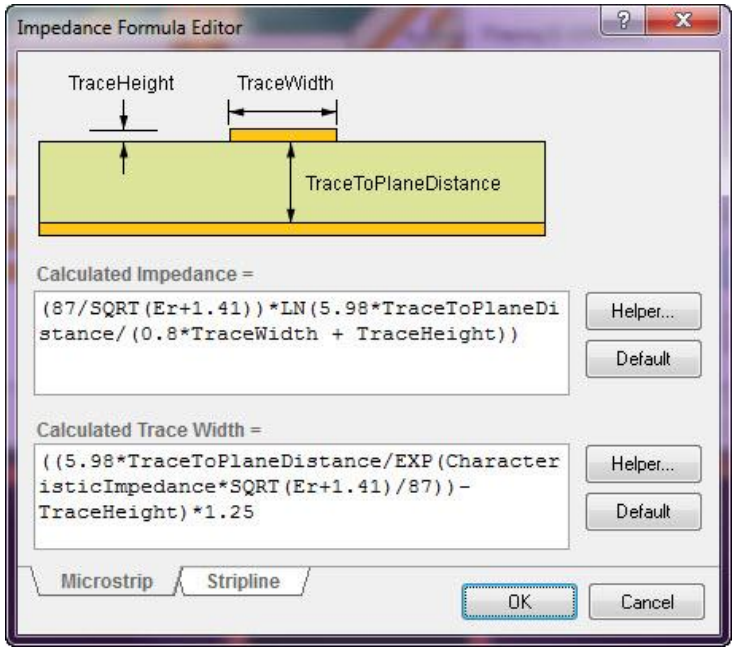
Setting the Rules on Schematics Level for a better design control



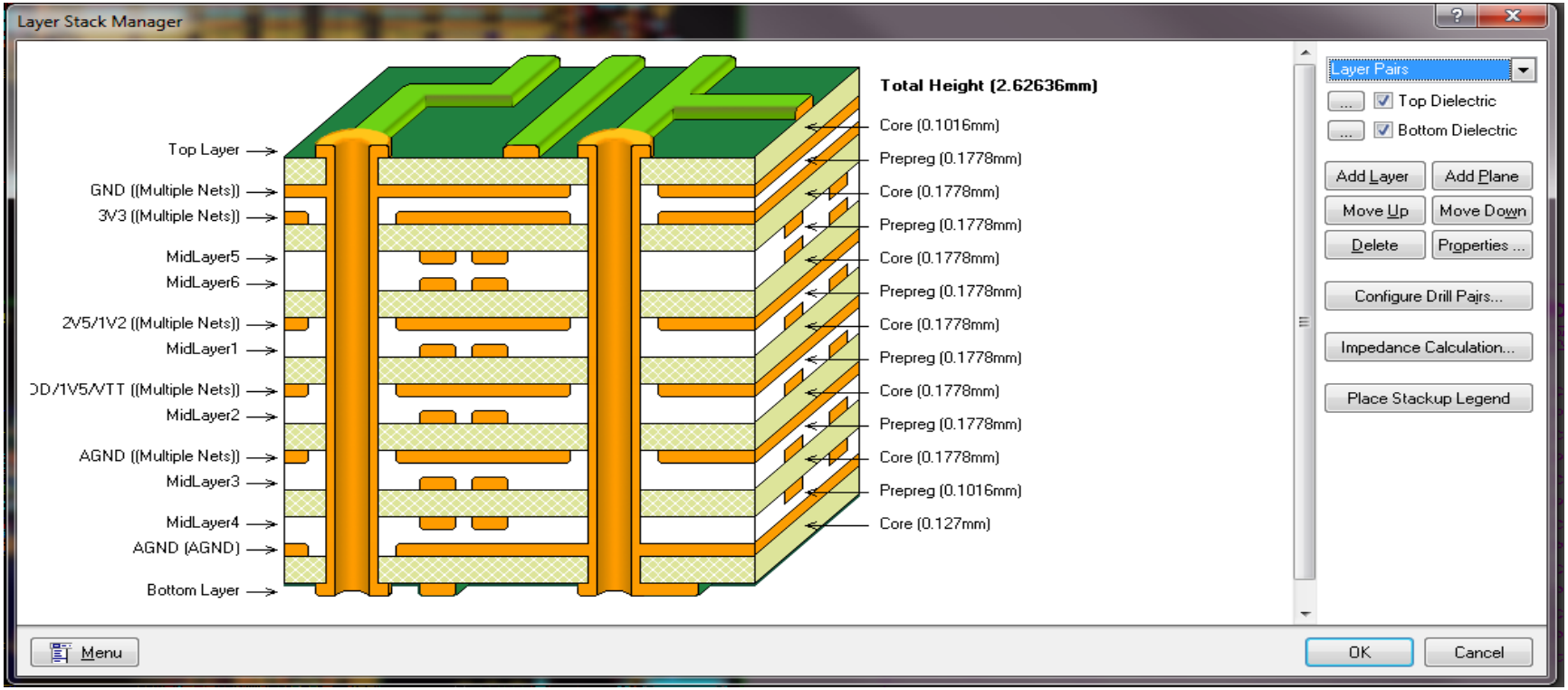








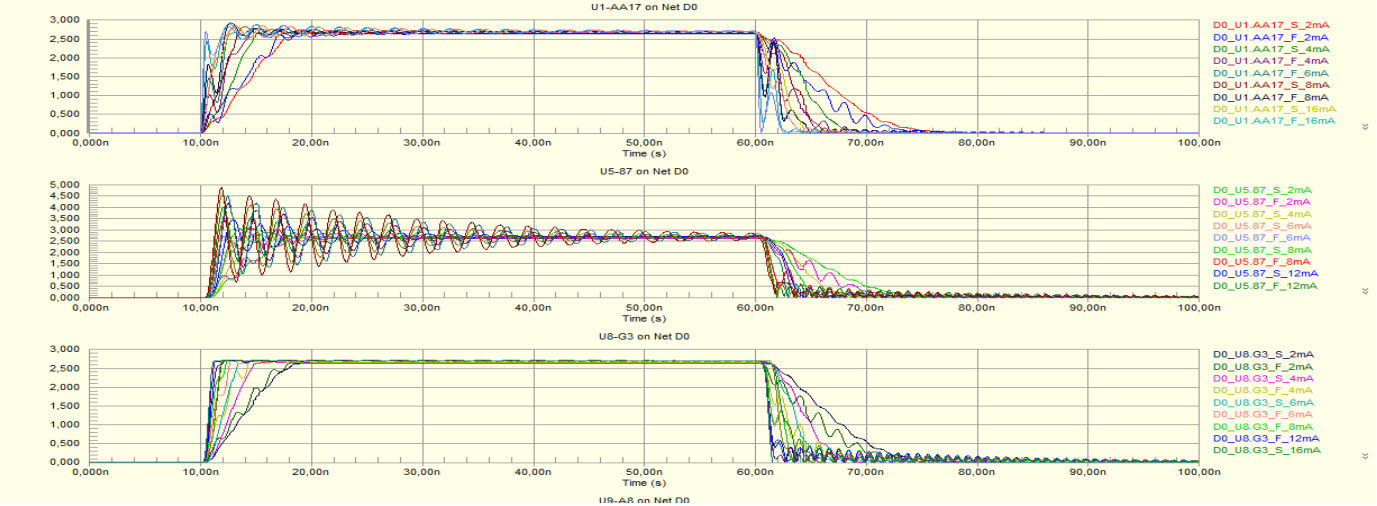
PCB Layer Stack Manager

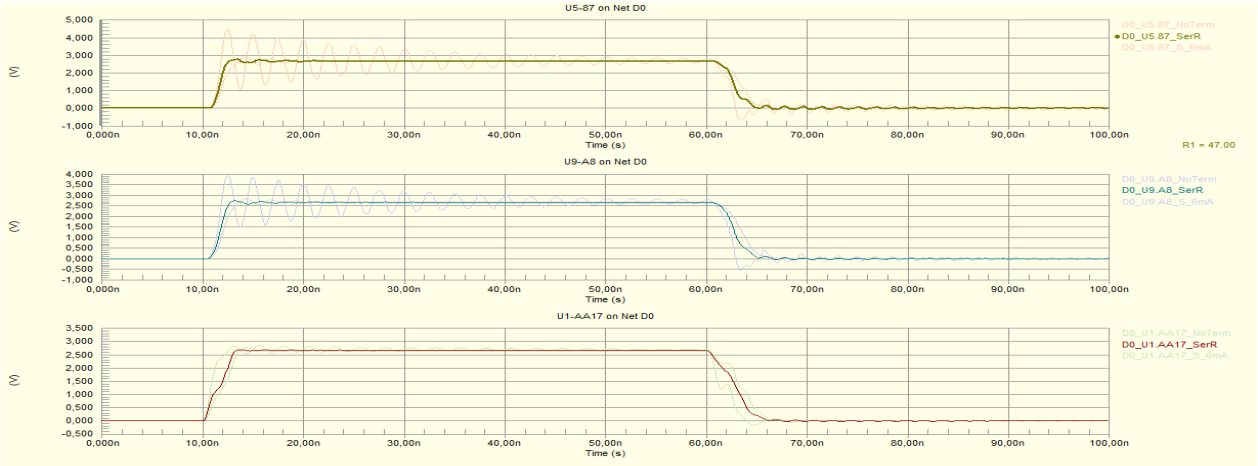


- Setting the Digital and Analog Layers
- Setting the Digital and Analog Power Plane

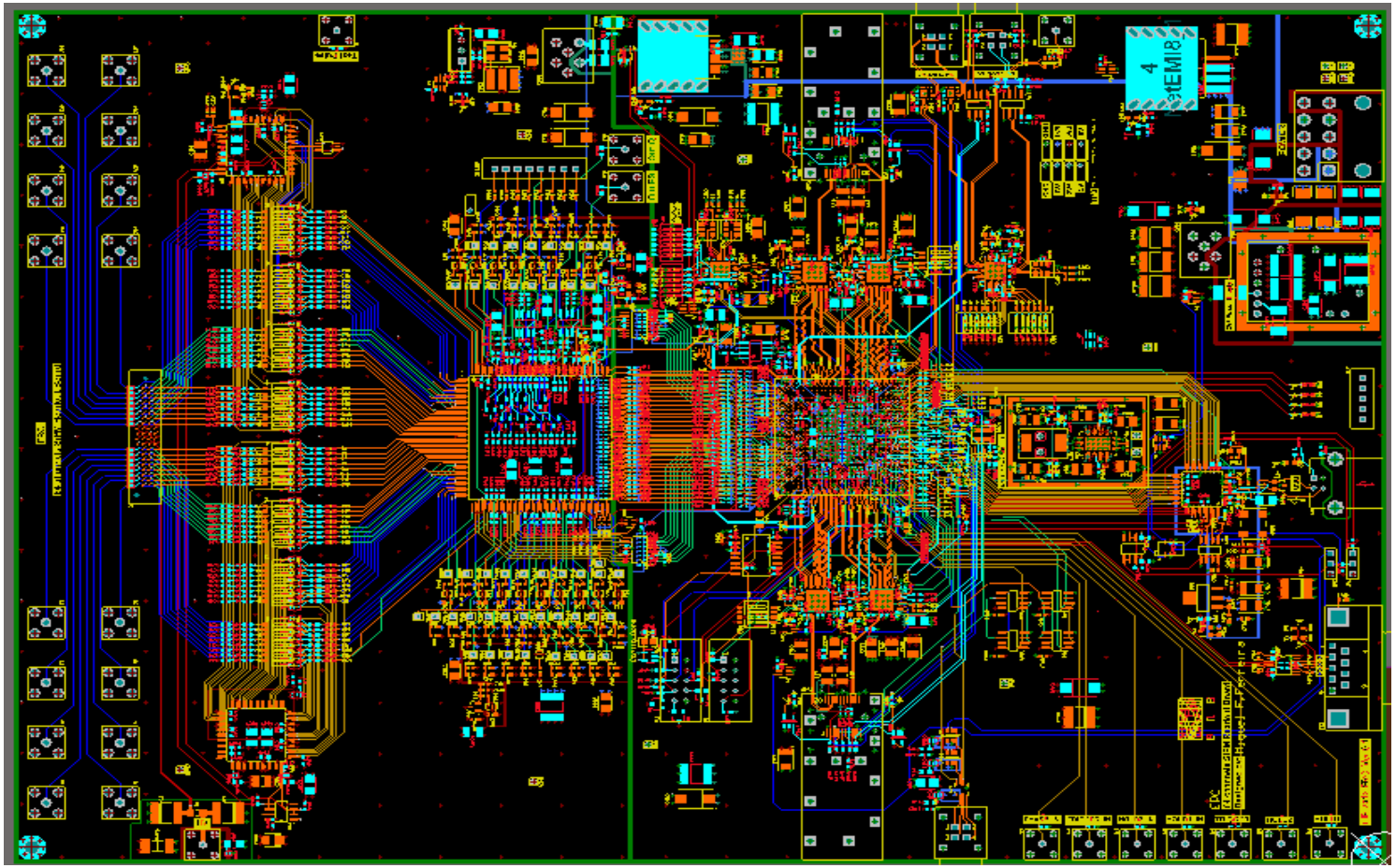
Signal Integrity Analysis

Bad termination Increases signal
Reflections which incraeses the overrall noise impact.





ERC Prototype Board Status and Plans



ERC Prototype Board Status and Plans

- Three PCB´s In production
- Assembly the Board over (1700 Components)

Thank you

Questions?