

ERC - Elementary Readout Cell



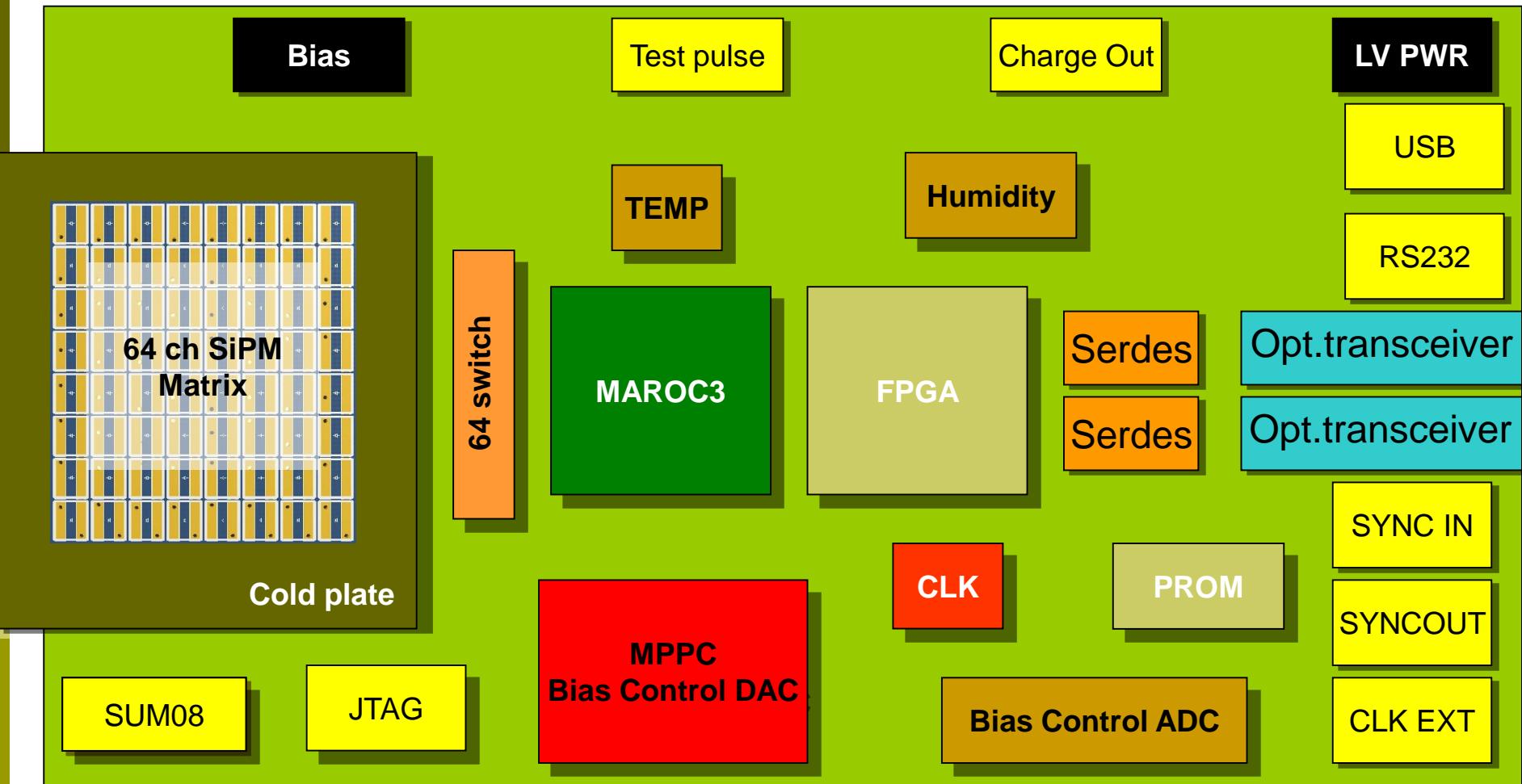
Miguel Ferreira

18th April 2012

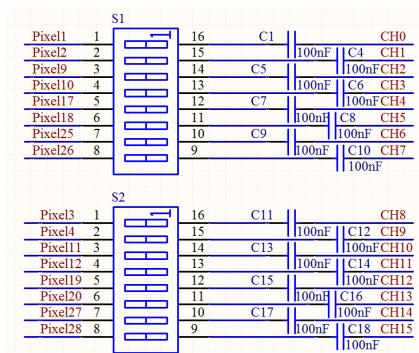
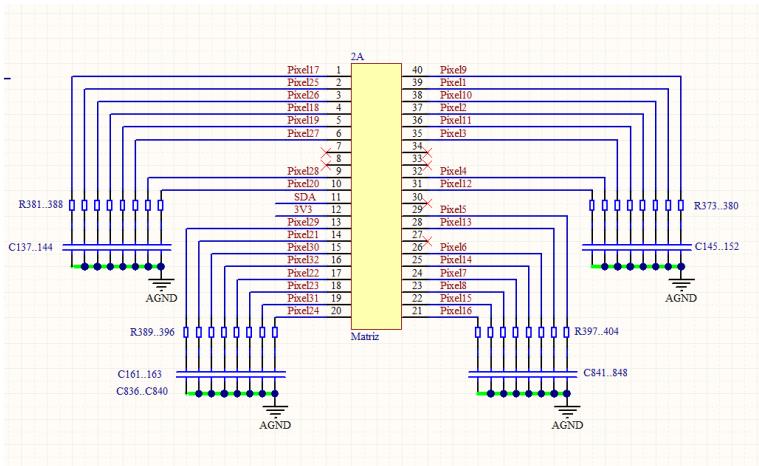
ERC Prototype Board

- MAROC3 chip (PQFP240 package)
- Altera Cyclone III (EP3C80F780C7N)
- LV regulation circuits (AVDD, VDD, VCIO, 3V3, 1V2,...)
- Bias supply regulation (DAC 14 Bits I2C)
- Bias supply monitoring (ADC I2C)
- 7 on-board sensors (TMP100 I2C)
- Internal CLK LVDS (125/60/40/80 MHZ)
- Humidity sensor (I2C)
- USB link (FPGA DATA OUT)
- 2 SFP Optical Link (FPGA DATA OUT)
- External CLOCK connector
- External SYNC connector
- External NIM TRIGGER connector
- JTAG Connector
- External ASIC output monitoring connectors (charge, SUM08)
- Internal ASIC test pulse (common to 64 channels)

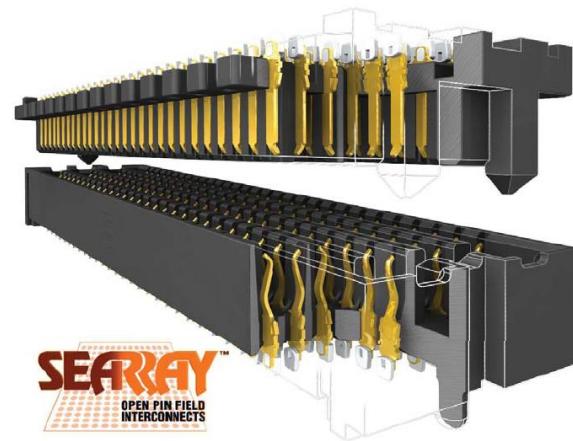
ERC Prototype Board



SiPM Analog Input with 50 ohm impedance control



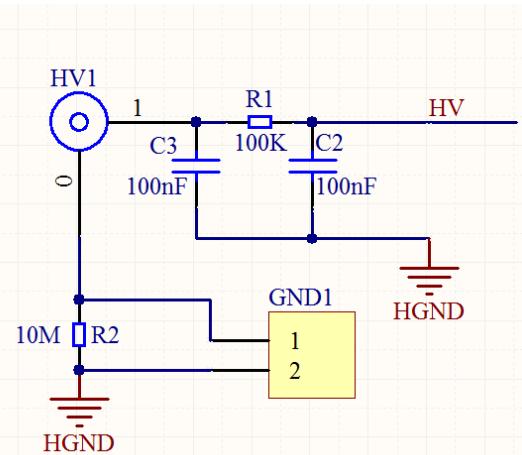
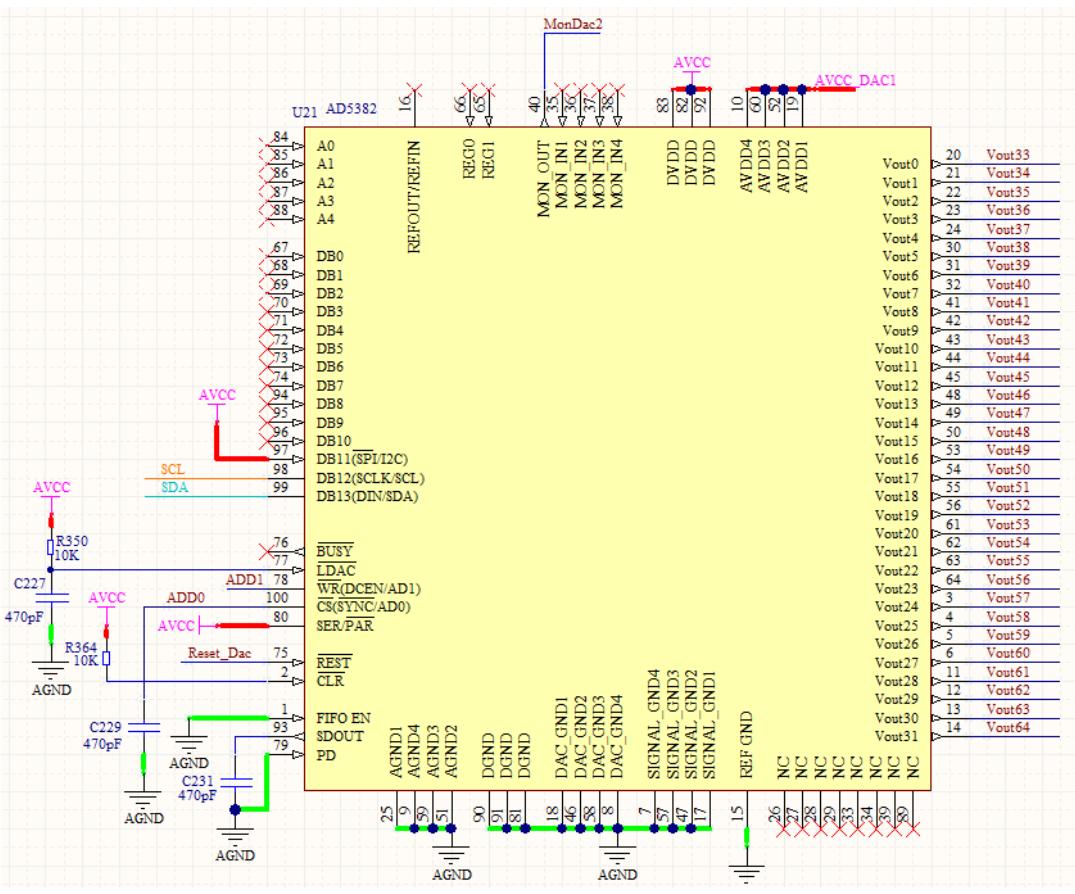
1A	IN<3>	out<2>	180 OUT CH2
CH3	1	IN<4>	179 OUT CH3
CH4	2	IN<5>	178 OUT CH4
CH5	3	IN<6>	177 OUT CH5
CH6	4	IN<7>	176 OUT CH6
CH7	5	IN<8>	175 OUT CH7
CH8	6	IN<9>	174 OUT CH8
CH9	7	IN<10>	173 OUT CH9
CH10	8	IN<11>	172 OUT CH10
CH11	9	IN<12>	171 OUT CH11
CH12	10	IN<13>	170 OUT CH12
CH13	11	IN<14>	169 OUT CH13
CH14	12	IN<15>	168 OUT CH14
CH15	13	IN<16>	167 OUT CH15
CH16	14	IN<17>	166 OUT CH16
CH17	15	IN<18>	165 OUT CH17
CH18	16	IN<19>	164 OUT CH18
CH19	17	IN<20>	163 OUT CH19
CH20	18	IN<21>	162 OUT CH20
CH21	19	IN<22>	161 OUT CH21
CH22	20	IN<23>	160 OUT CH22
CH23	21	IN<24>	159 OUT CH23
CH24	22	IN<25>	158 OUT CH24
CH25	23	IN<26>	157 OUT CH25
CH26	24	IN<27>	156 OUT CH26
CH27	25	IN<28>	155 OUT CH27
CH28	26	IN<29>	154 OUT CH28
CH29	27	IN<28>	153 OUT CH29



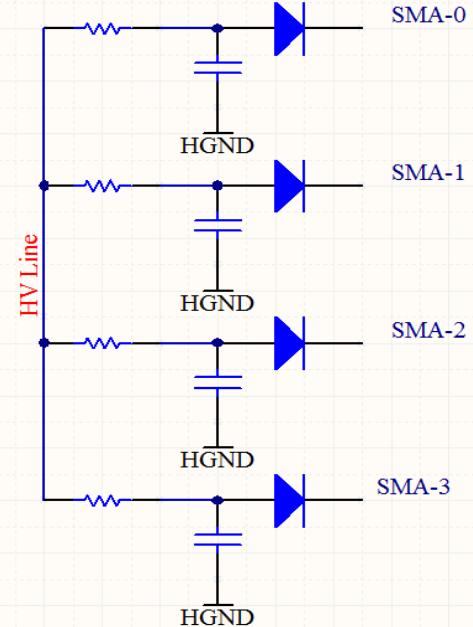
SEARAY™
OPEN PIN FIELD
INTERCONNECTS

HV Regulation & Distribution

5 volts range with a 0.3mV LSB



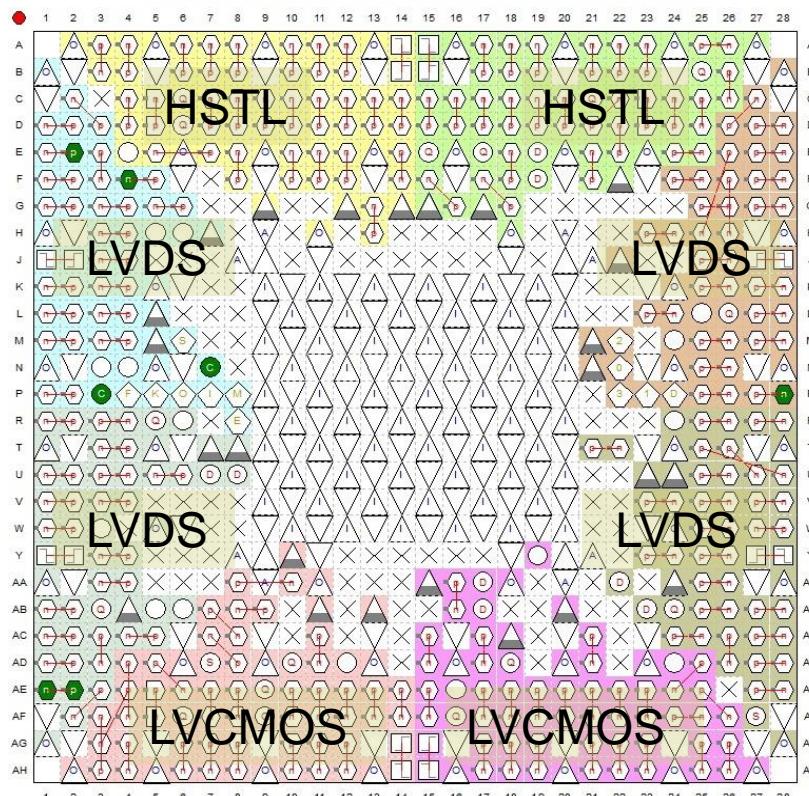
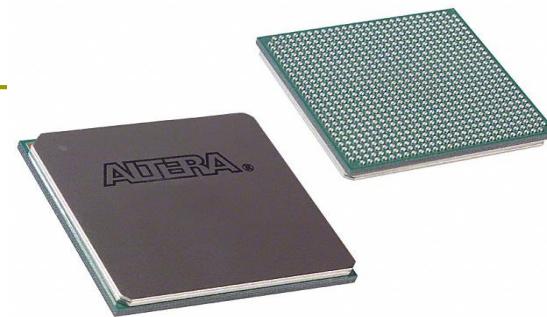
SiPM Array



Cyclone III FPGA

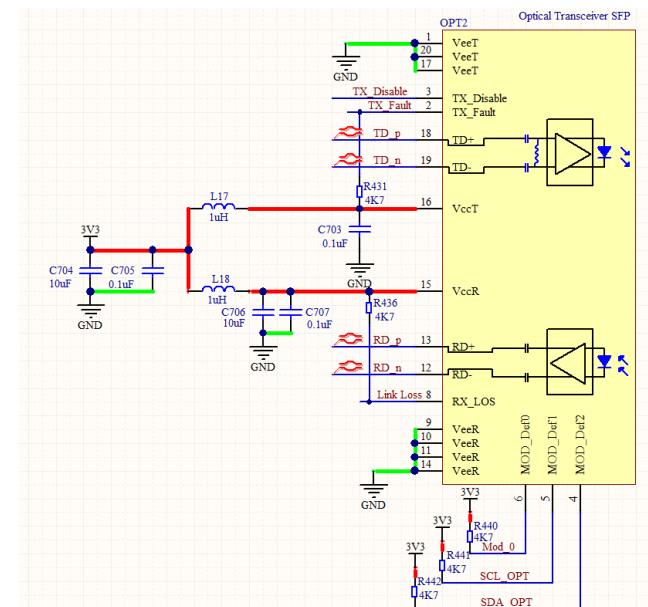
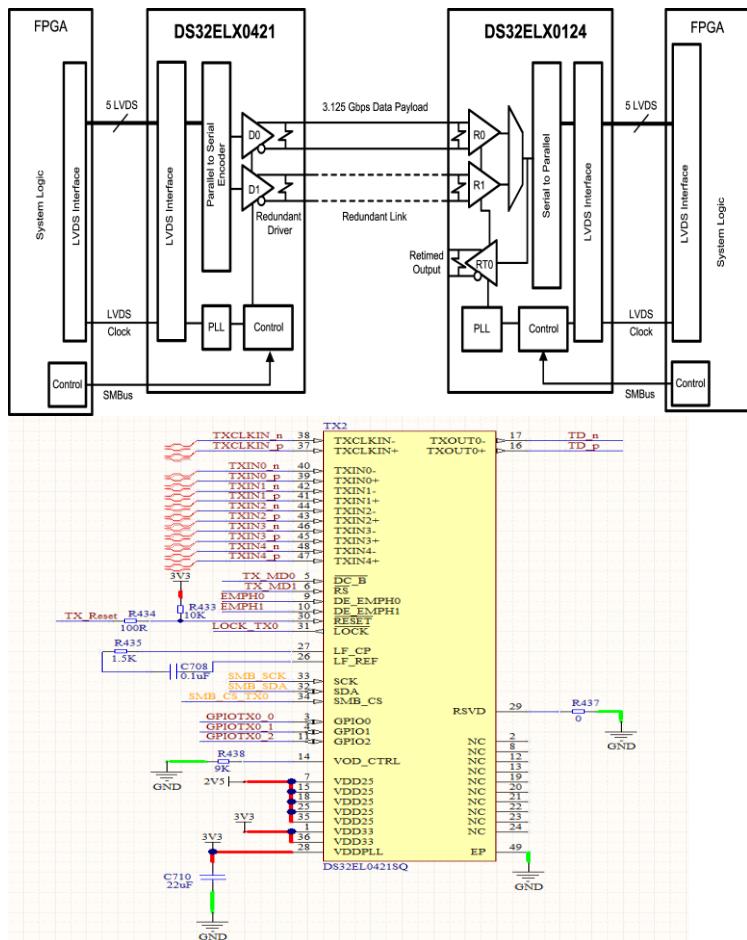
Quantity	Item Number	Customer Reference	
	EP3C80F780C7N		Add to Order

Datasheets		Cyclone III Brochure Cyclone III FPGA Family Errata Cyclone III Datasheet Cyclone III Design Guidelines Cyclone III Family Overview Cyclone III Device Handbook Vol2
Product Photos		780-FBGA Pkg
Standard Package		36
Category		Integrated Circuits (ICs)
Family		Embedded - FPGAs (Field Programmable Gate Array)
Series		Cyclone® III
Number of Logic Elements/Cells		81264
Number of LABs/CLBs		5079
Total RAM Bits		2810880
Number of I / O		429
Number of Gates		-
Voltage - Supply		1.15 V ~ 1.25 V
Mounting Type		Surface Mount
Operating Temperature		0°C ~ 85°C
Package / Case		780-FBGA
Supplier Device Package		*
Other Names		544-2524
Lead Free Status		Lead free
RoHS Status		RoHS Compliant

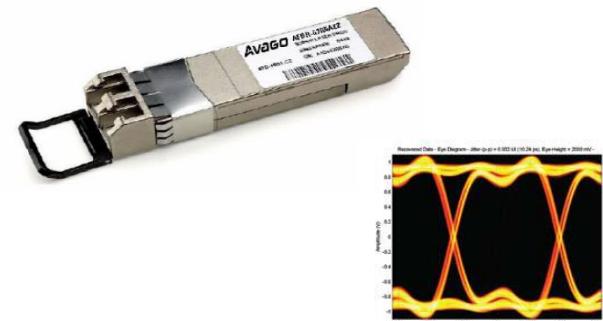


Optical Link up to 3.125Gbps

Transceiver from National Semiconductor



Digital Diagnostic SFP, 850 nm, 4.25/2.125/1.0625



ERC Schematics Layout

Setting the Rules on Schematics Level for a better design control

The schematic shows a DS32ELX0421SQ chip (U1) with several pins labeled:

- TXCLKIN- (pin 38)
- TXCLKIN+ (pin 37)
- TXIN0- (pin 40)
- TXIN0+ (pin 39)
- TXIN1- (pin 42)
- TXIN1+ (pin 41)
- TXOUT1_EN (pin 12)
- TXOUT0- (pin 17)
- TXOUT0+ (pin 16)
- TXOUT1- (pin 20)
- TXOUT1+ (pin 19)

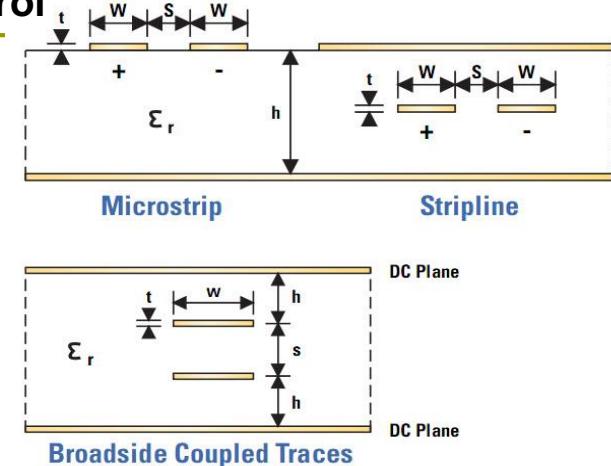
A parameters dialog box is open, showing the following settings:

Name	DIFFPAIR
X-Location	1050
Orientation	0 Degrees
Y-Location	940
Locked	<input type="checkbox"/>

Properties table:

Visible	Name	Value	Type
<input checked="" type="checkbox"/>	DifferentialPair	True	STRING
<input type="checkbox"/>	Rule	Matched Net Lengths [Tolerance = 0.1mm]	STRING
<input checked="" type="checkbox"/>	Rule	Impedance Constraint [Min = 100.0 Max = 100.0]	STRING
<input checked="" type="checkbox"/>	Rule	Parallel Segment Constraint [Gap = 0.127mm Limit = 2.54mm]	STRING

Buttons at the bottom: Add..., Remove..., Edit..., Add as Rule..., OK, Cancel.



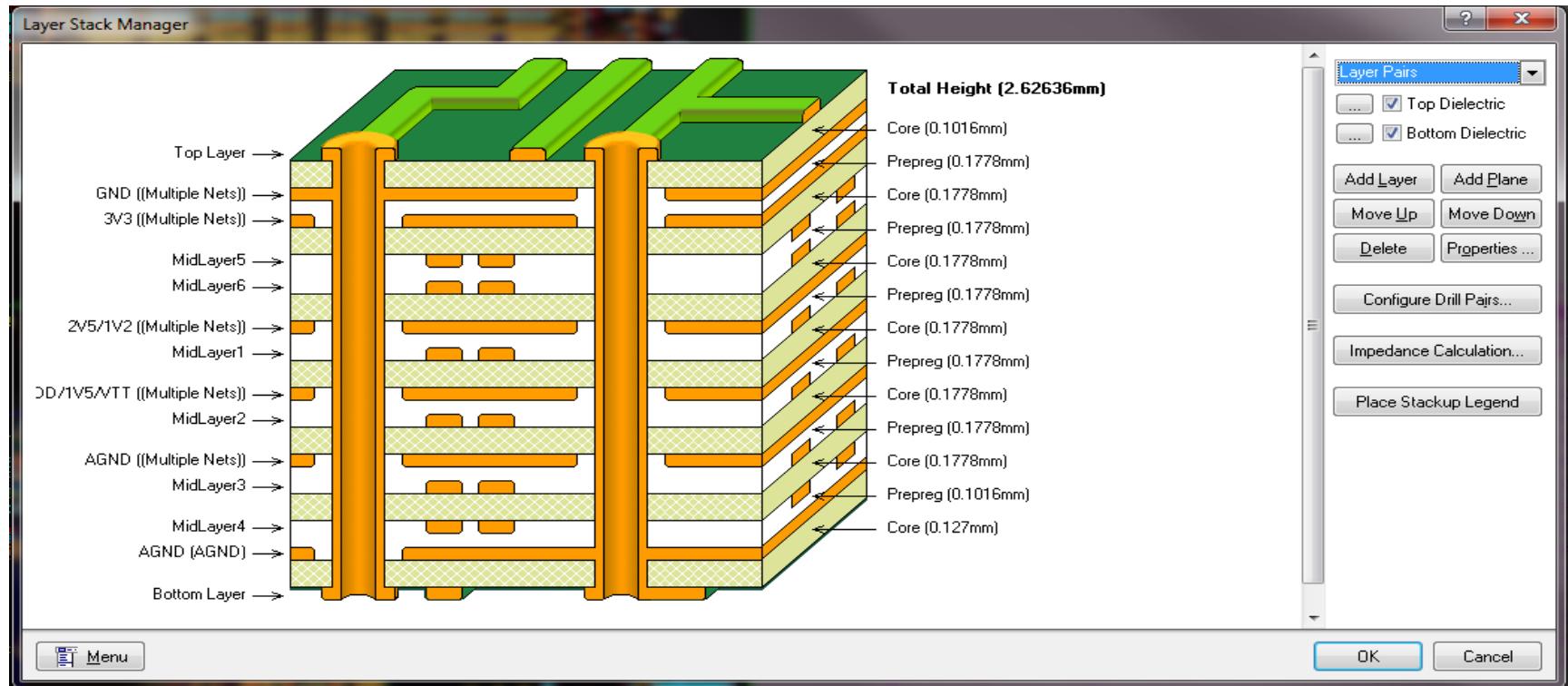
Impedance Formula Editor dialog box:

Calculated Impedance =
$$(87/\text{SQRT}(\epsilon_r+1.41)) * \text{LN}(5.98 * \text{TraceToPlaneDistance} / (0.8 * \text{TraceWidth} + \text{TraceHeight}))$$

Calculated Trace Width =
$$((5.98 * \text{TraceToPlaneDistance}) / \text{EXP}(\text{CharacteristicImpedance} * \text{SQRT}(\epsilon_r+1.41) / 87)) - \text{TraceHeight} * 1.25$$

Buttons: Microstrip, Stripline, OK, Cancel.

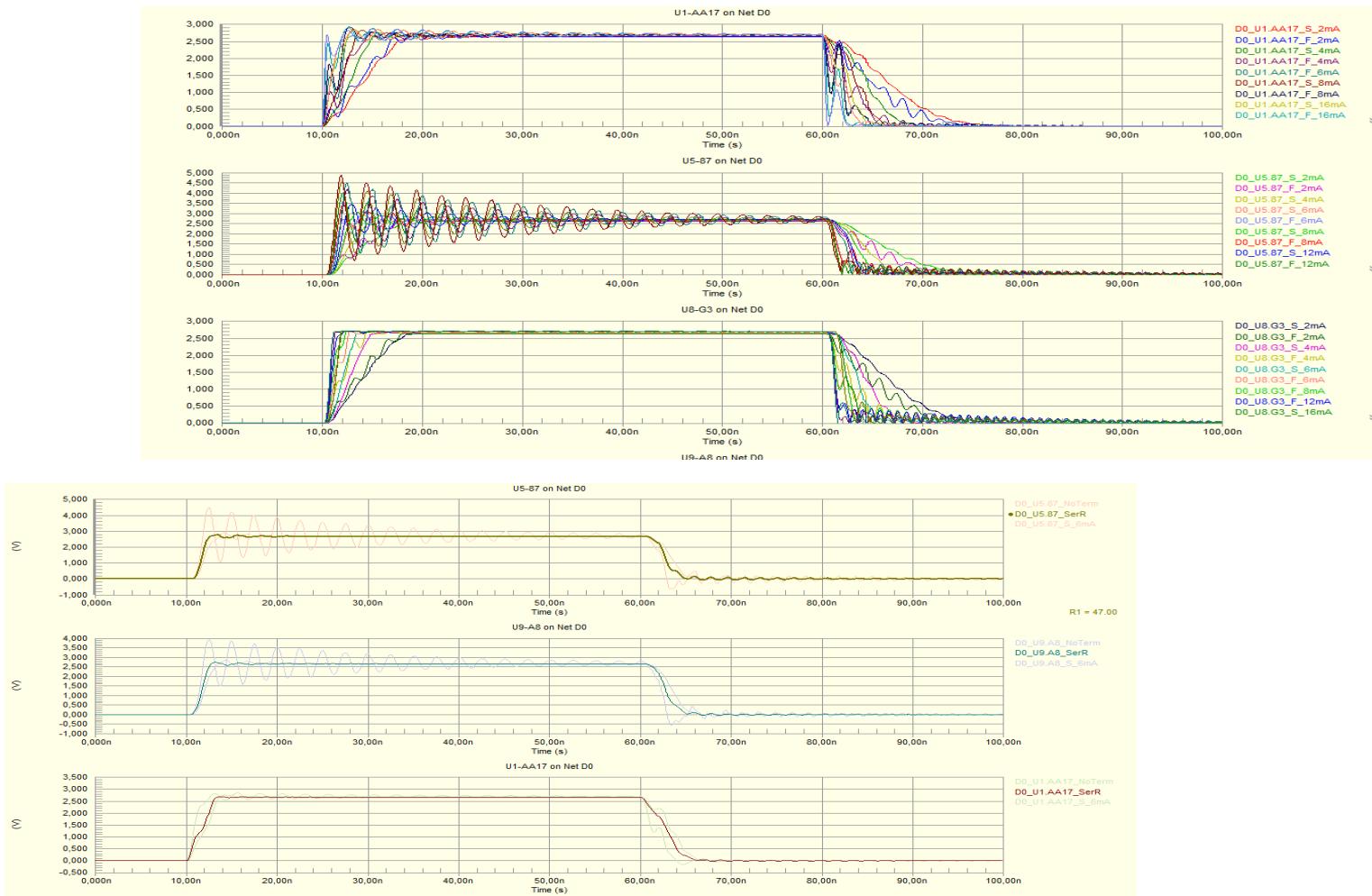
PCB Layer Stack Manager



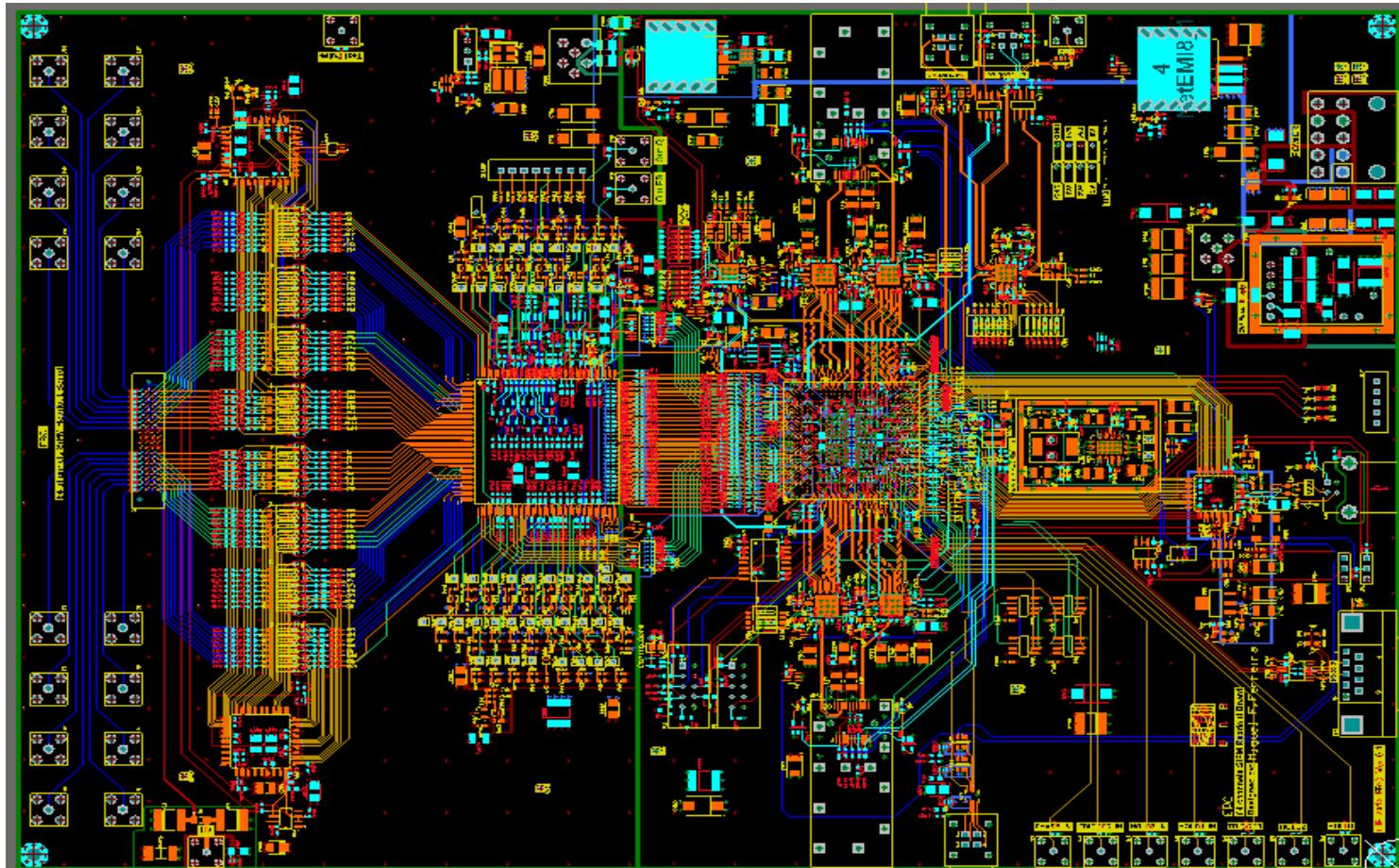
- Setting the Digital and Analog Layers
- Setting the Digital and Analog Power Plane

Signal Integrity Analysis

Bad termination Increases signal reflections which increases the overall noise impact.



ERC Prototype Board Status and Plans



ERC Prototype Board Status and Plans

- Three PCB's In production
- Assembly the Board over (1700 Components)

Thank you

Questions?