Front-end electronics for hybrid and monolithic particle detectors: new ideas and technologies

Lodovico Ratti
(lodovico.ratti@unipv.it)

Dipartimento di Ingegneria Industriale e dell'Informazione
Università degli Studi di Pavia
and INFN Pavia

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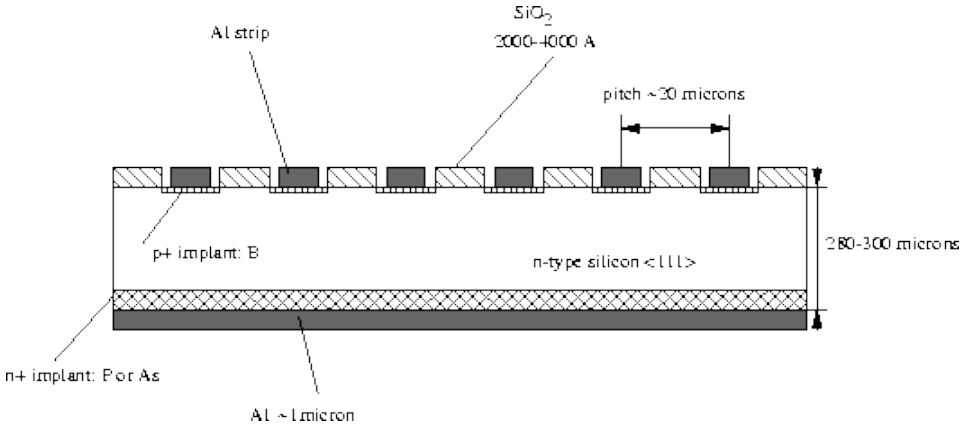
Outline

- Generalities on readout electronics (mostly) for pixel detectors: signal processing, readout chip floorplan, interconnection, technologies
- Enabling technologies for advanced pixel detectors: evolution of technologies for readout chips, CMOS technologies, vertical integration
- Some examples of advanced pixel detector design

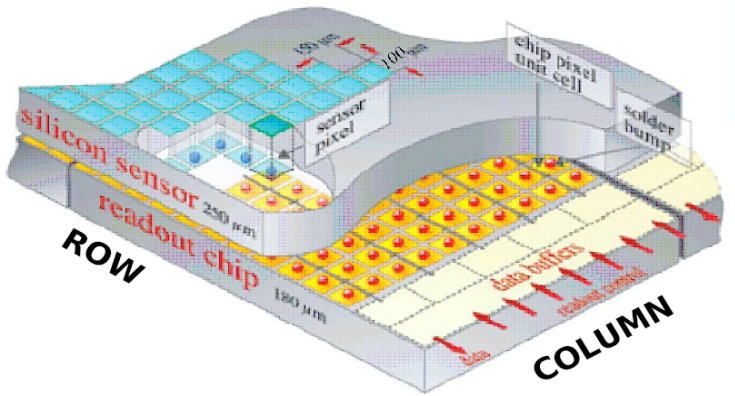
Radiation detectors

- Radiation detection systems may be used to measure
  - the amount of energy released by a particle (a charged one, or a photon) while passing through the sensor volume
  - the position (in one or two dimensions) of a particle passing through the surface of a detector (to be intended as a set of sensors with a given geometrical arrangement)
  - the time of arrival of a particle
  - the number of particles hitting the detector, or the total energy released by those particles in a given position
- Semiconductor microstrip and pixel detectors are used to measure the position of a particle hitting the detector surface (they are also called position-sensitive detectors)

Microstrip detectors



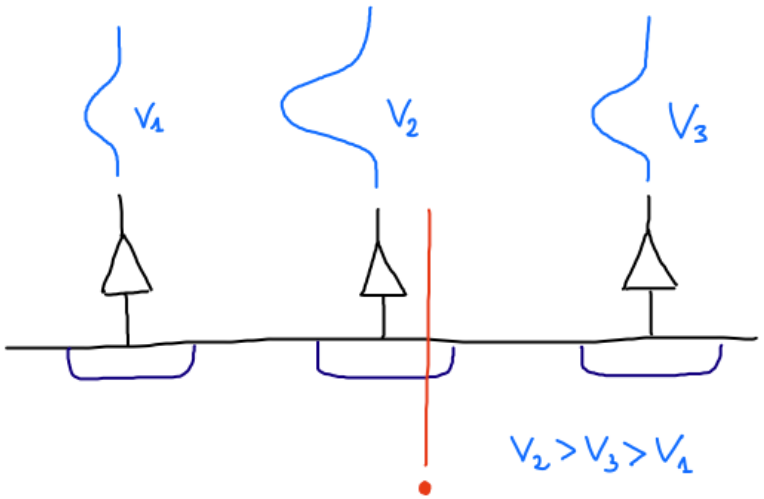
Pixel detectors



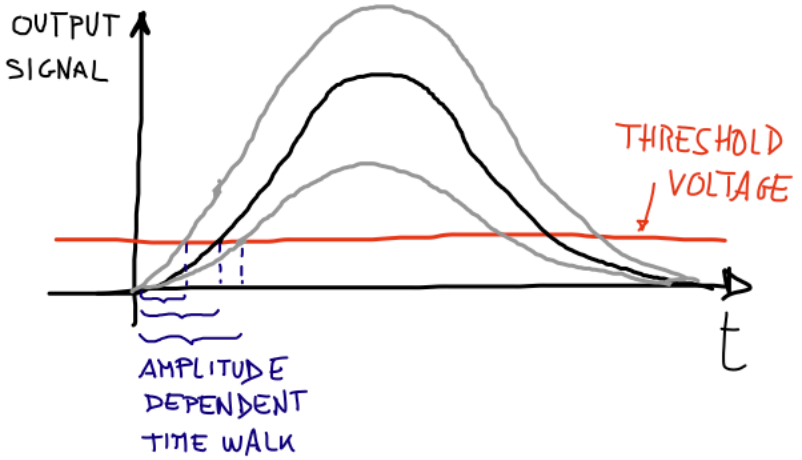
Analog signal processing

- Depending on the application and on the required spatial resolution, semiconductor microstrip and pixel detectors, together with the relevant readout electronics, may be required to provide also information on the amount of energy the particle has released in the sensor volume (amplitude measurement)
- The signal from a capacitive detector is first read out by an analog processing channel, which in its optimum version includes a charge preamplifier and a shaper for signal-to-noise ratio optimization
- A discriminator is generally used to compare the signal at the shaper output to a preset threshold voltage, therefore providing information about the presence of an interesting event (hit/no hit information)

Center of mass of a cluster



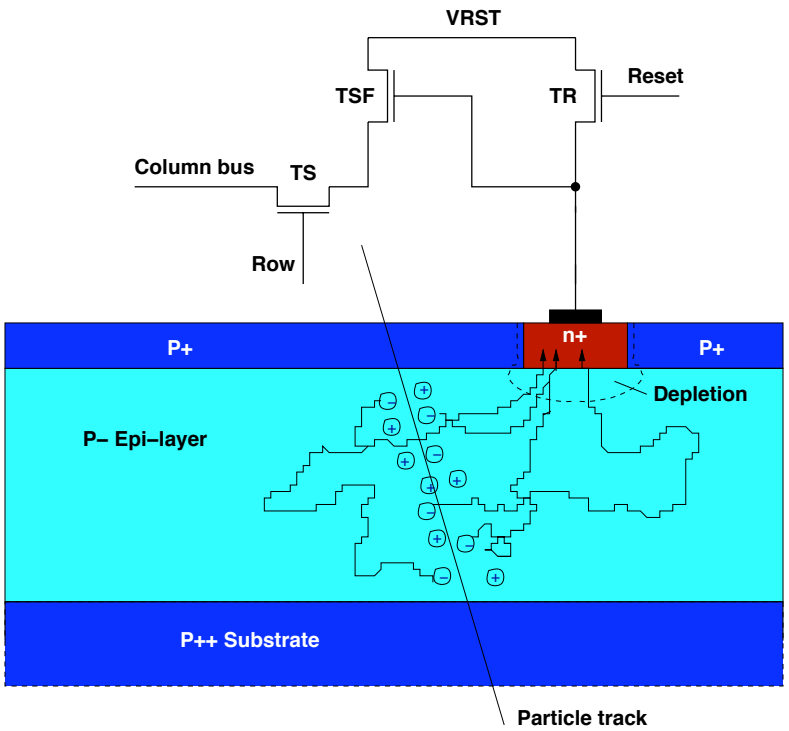
Hit time calculation



Readout architectures

- The digital hit signal at the discriminator output must be further processed by circuitry in the pixel or at the chip periphery; processing may just involve reading out the single hit/no hit bit of information or using it to perform more complex operations
- Choice of the set of operations to be performed on the data collected in a detector before sending them out (implemented in the readout architecture) depends on the target application
- Also the design approach (hybrid vs monolithic) and the available technology may impact on the design of the readout chip; evolution (scaling down) of CMOS technologies and, in general, of microelectronic processes (vertical integration) may help improve performance and include more functionalities in the readout circuits

Monolithic sensor



Functionalities and intelligence

- The task of the front-end is measuring the charge delivered by a capacitive source with the best accuracy compatible with the intrinsic noise of the readout circuit and with the constraints set by the application

noise – power – speed - area

- Finding the best compromise may imply using additional blocks (in the pixel or at the chip level), adding functionalities, extend the set of operations performed on chip

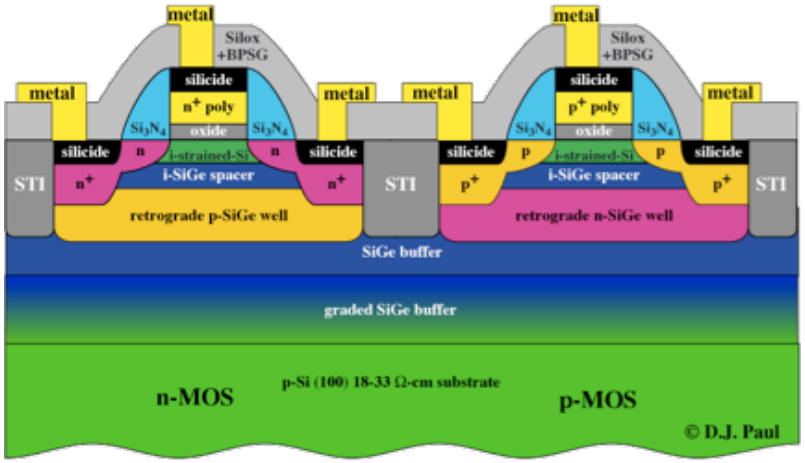
- On-chip intelligence generally includes the set of functions performed directly on data, inside the pixel, at the chip level or in a more complicated chip assembly: A-to-D conversion, zero suppression, data sparsification, buffering, encoding, lossless compression, error correction, serialization, track discrimination, histogramming

- Other blocks, not necessarily acting on the signal, are used to improve the performance of the in-pixel readout channel or of the chip as a whole, for example by adjusting or calibrating some parameters or by transferring to the chip what was previously done outside: threshold correction circuits, gain calibration, polarity selection, baseline restoration, DC-DC conversion, clock generation, I/O communication, logic level conversion

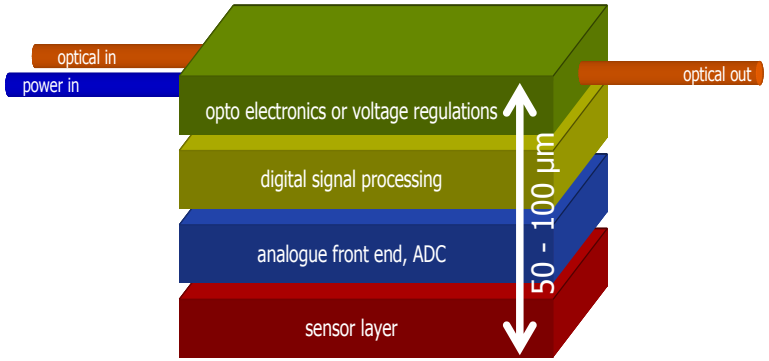
Application needs and technologies

- The driving force for the increasing functional density of readout chips for radiation detectors is given by the need for:
  - higher granularity (smaller pileup, capability for track separation)
  - higher speed (capability for processing hits at a higher rate)
  - data reduction (to limit the bandwidth requirements for transmission to DAQ)
  - higher degree of radiation hardness
- The advance in readout chip design is mainly enabled by
  - evolution of CMOS processes
  - development of interconnection techniques and vertical integration technologies

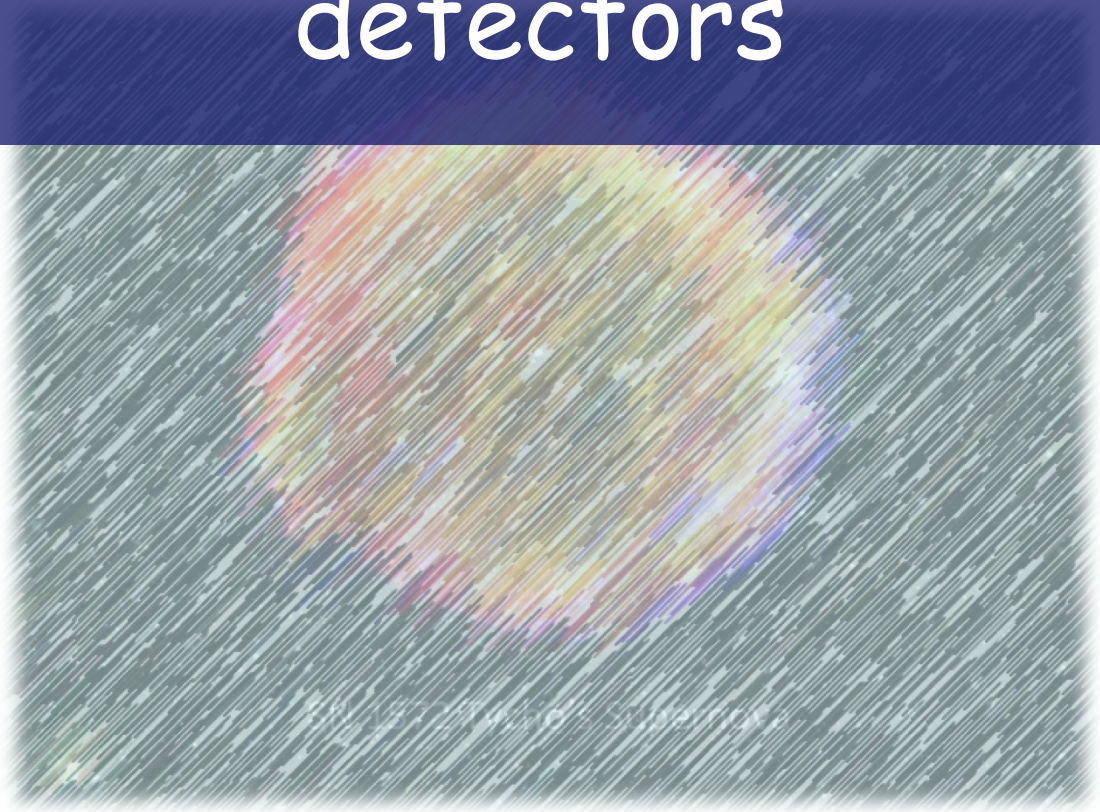
CMOS technology



3D integration

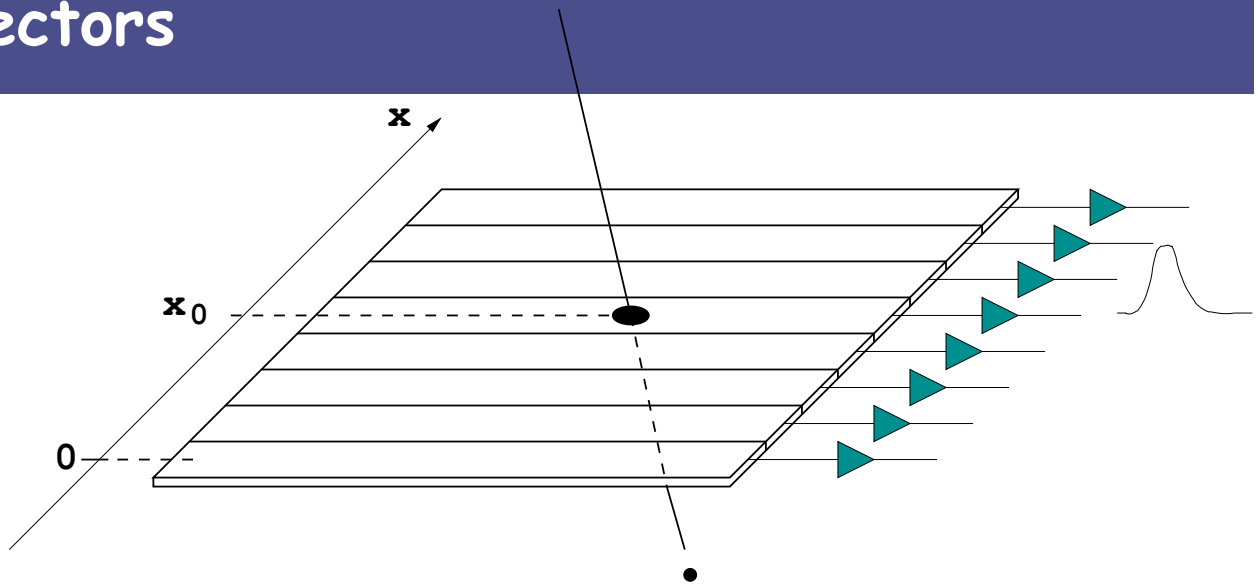


Generalities on readout electronics for radiation detectors

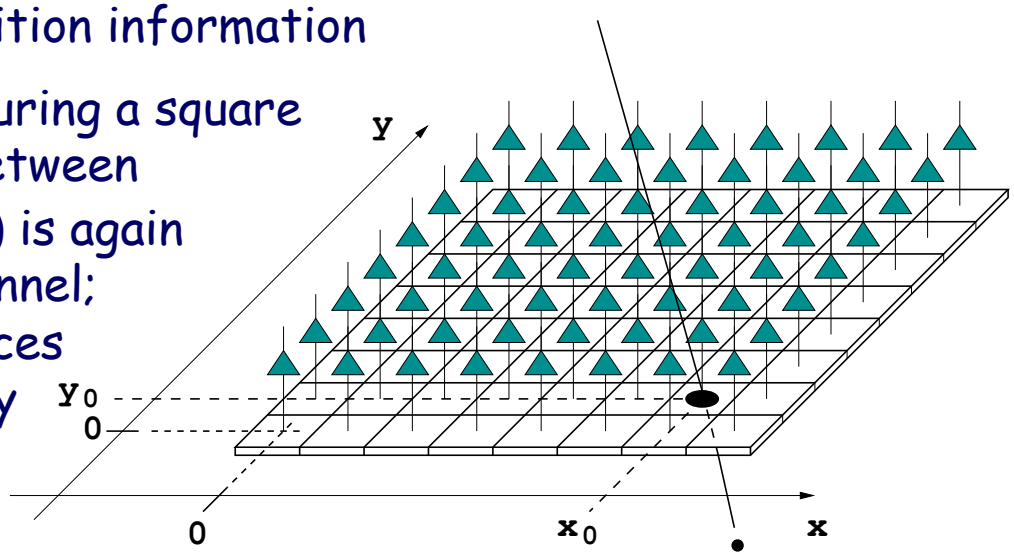


Microstrip and pixel detectors

- In a microstrip detector, each sensor element has the shape of an elongated strip (up to a few cm long) and is read out by a dedicated processing channel; readout channels are arranged in arrays of several tens or hundreds of elements; typical pitch is in the order of a few tens of μm up to 100 μm; a microstrip detector provides monodimensional position information

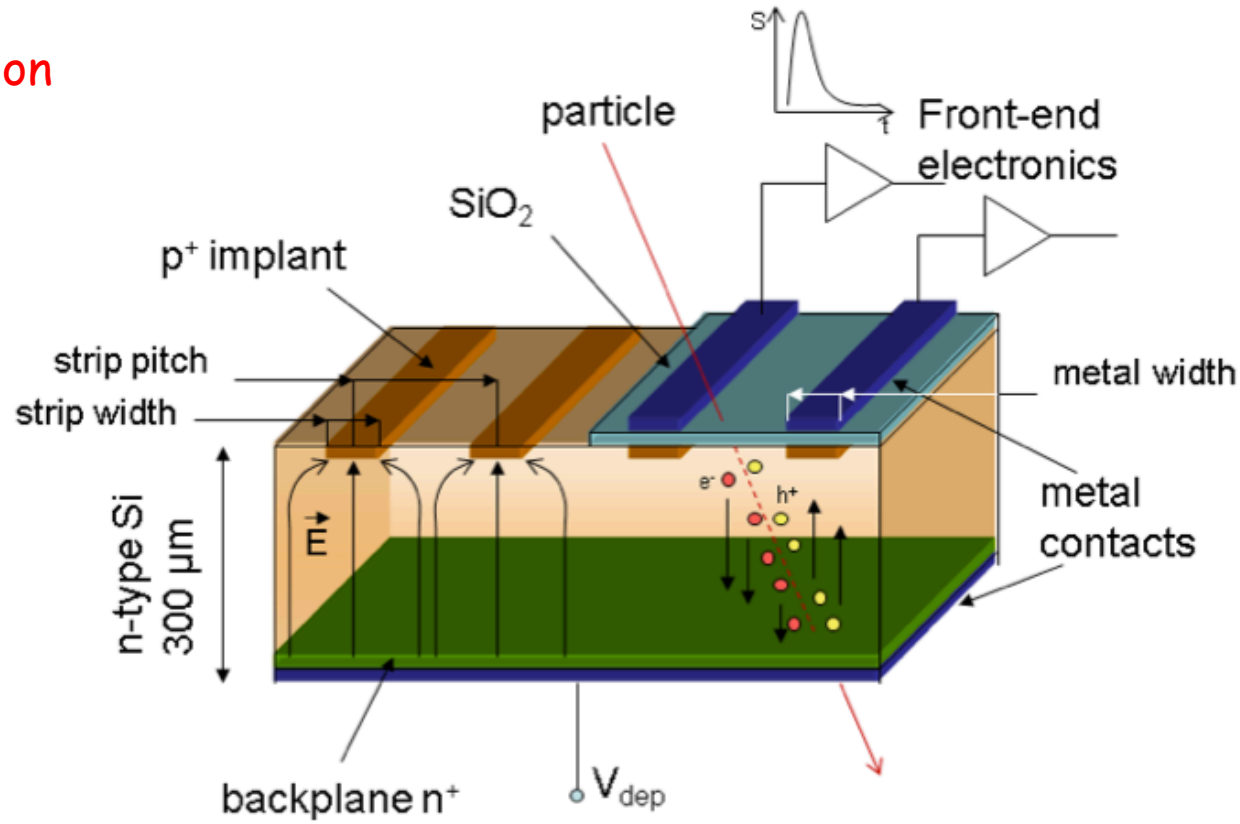


- In a pixel detector, each element, featuring a square or rectangular shape (pitch may vary between several tens and a few hundreds of μm) is again read out by a dedicated processing channel; readout channels are arranged in matrices including a few thousands of elementary cells; a pixel detector provides bidimensional position information



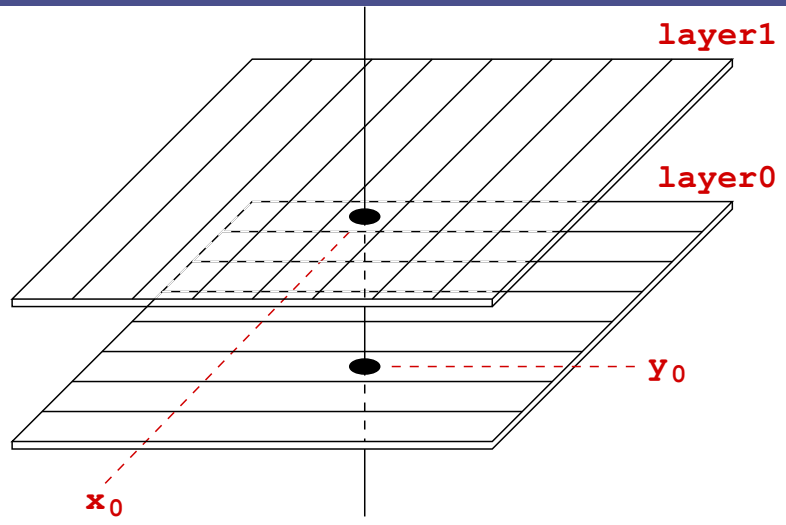
Detectors in high resistivity silicon

- In a microstrip, a large area diode is divided into many small regions, readout separately; production of strip detectors may follow the method of planar diodes using the somewhat more complicated geometrical strip structure
- Each small strip diode consists of a shallow p+ region on a very lowly doped n- substrate
- Full depletion and almost complete and fast collection of the charge released in the sensor substrate may be achieved by applying a reverse voltage of a few tens to a hundred volts



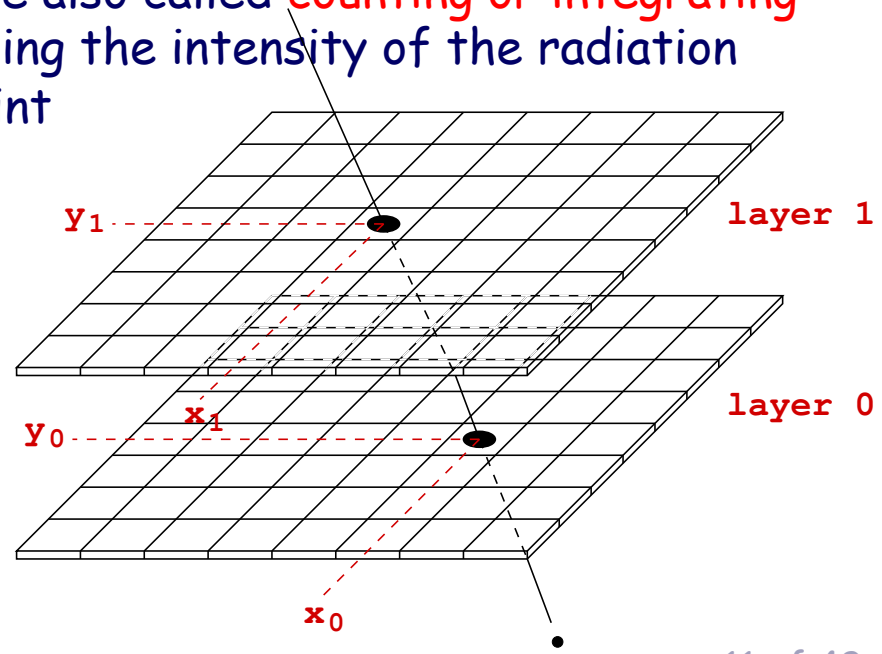
Position and momentum measurement

- A double microstrip detector layer may be used to obtain bidimensional information on the position of the impinging particle (also double-sided microstrip detectors are available)



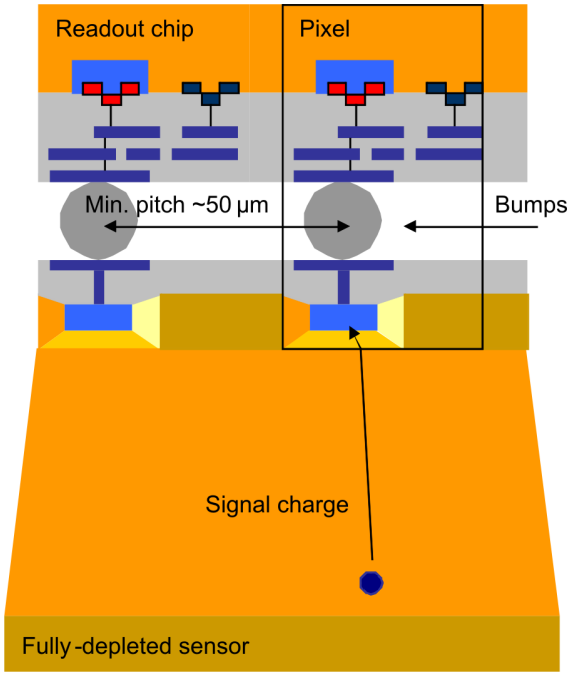
- A single pixel detector layer is sufficient in imaging applications, where the detector has to count the number of striking particles (typically photons, these are also called counting or integrating detectors) in each element, therefore providing the intensity of the radiation hitting the detector surface at any single point

- A double pixel detector layer may be used to obtain information on the momentum (in particular, the direction) of the impinging particle; tracking detectors usually employ multiple layers to improve resolution



Hybrid and monolithic approach

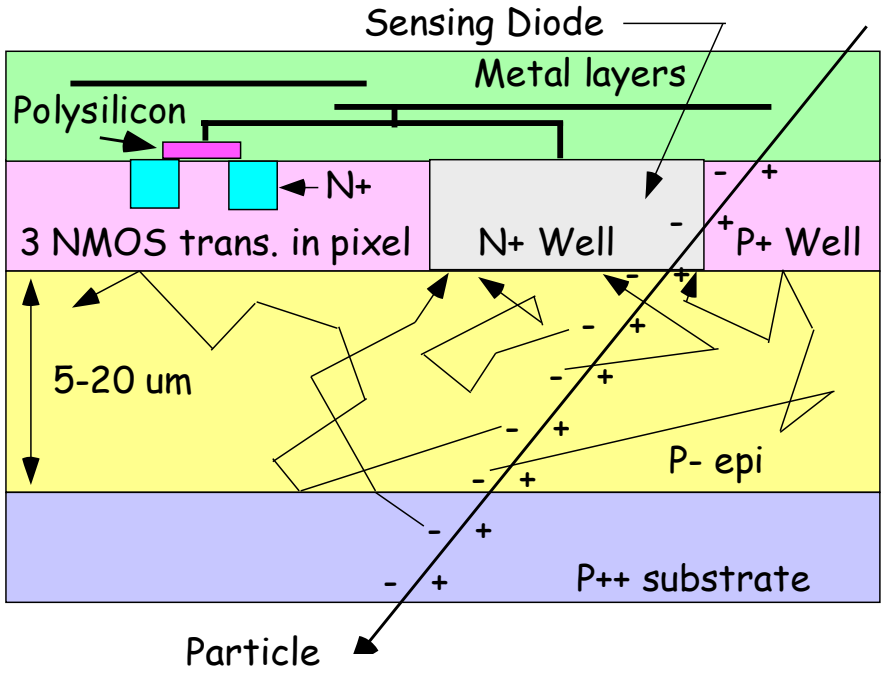
- In semiconductor microstrip and pixel detectors, each microstrip or pixel is read out by a processing channel which generally includes both analog and logic blocks
- In most cases, front-end electronics is integrated in a different piece of silicon from the detector; actually processes for detector fabrication (detector-grade) are quite different from processes for fabrication of microelectronic circuits (electronics-grade)
- Detector and front-end electronics have to be externally interconnected; microstrip detectors are typically connected to the front-end electronics through wire bonding techniques; bump bonding is instead the mainstream technology for pixel detector-to-electronics interconnection



- Sometimes, detectors are monolithically integrated with the front-end electronics; a choice has to be made, in this case, between electronics-grade processes (with possible limitations to the detector performance) and detector-grade processes (with possible degradation in the front-end electronics properties)

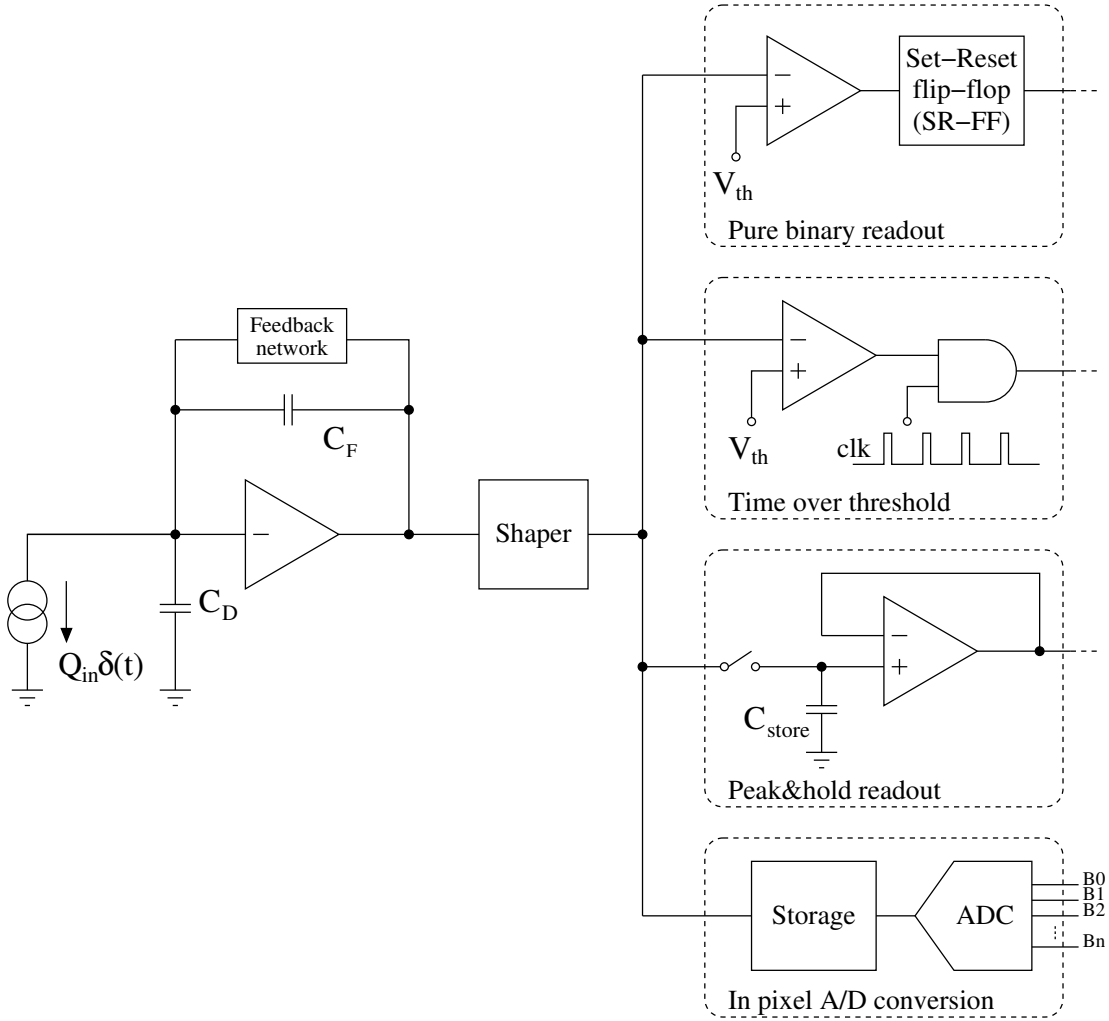
CMOS monolithic sensors

- CMOS MAPS operation is based on the presence of a (relatively) high resistivity (about 10 to 1000 Ω•cm) epitaxial layer, 5 to 20 µm thick (available in so called opto technologies); they are widely used as imaging devices in the visible spectrum; their operation have been adapted to particle tracking in high energy physics experiments and electron microscopy
  - The impinging particle releases electron-hole pairs along its track and, in particular, in the epitaxial layer; this holds also for photons in the visible spectrum, which simply have a shorter range in silicon
  - The epitaxial layer, which is sandwiched between the low resistivity substrate and surface P+ wells, acts as a potential well; therefore, the charge released in the epitaxial layer is confined in the region and can diffuse to one of the N+ collecting electrodes (at least the fraction of charge which does not recombine)



Hit information processing

- Once a hit has been detected, amplitude analog information at the shaper output can be retrieved in one of four possible ways



Pure binary readout; analog information is discarded, just hit/no hit information is provided by the readout chip for each channel

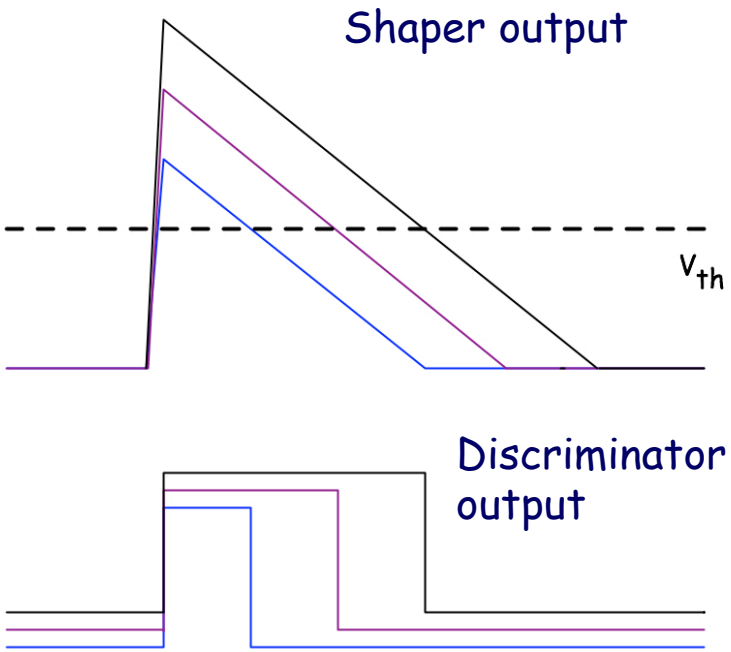
Time over Threshold (ToT); amplitude is converted to a time duration by comparing the shaper output to a preset threshold

Peak & hold; peak voltage at the shaper output is sampled and transferred to the chip periphery

In-pixel A/D conversion; peak voltage at the shaper output is sampled, converted to a digital word and transferred to the chip periphery

Time over Threshold (ToT)

- The Time over Threshold (ToT) technique provides a direct amplitude-to-time conversion; the signal at the shaper output is compared to a fixed voltage at the input of a threshold discriminator; the signal at the output of the discriminator is a digital pulse, whose duration is equal to the time during which the signal at the shaper output exceeds the threshold; digitization is easily achieved by computing the logic AND between the discriminator pulse and a reference clock and by counting the number of clock pulses

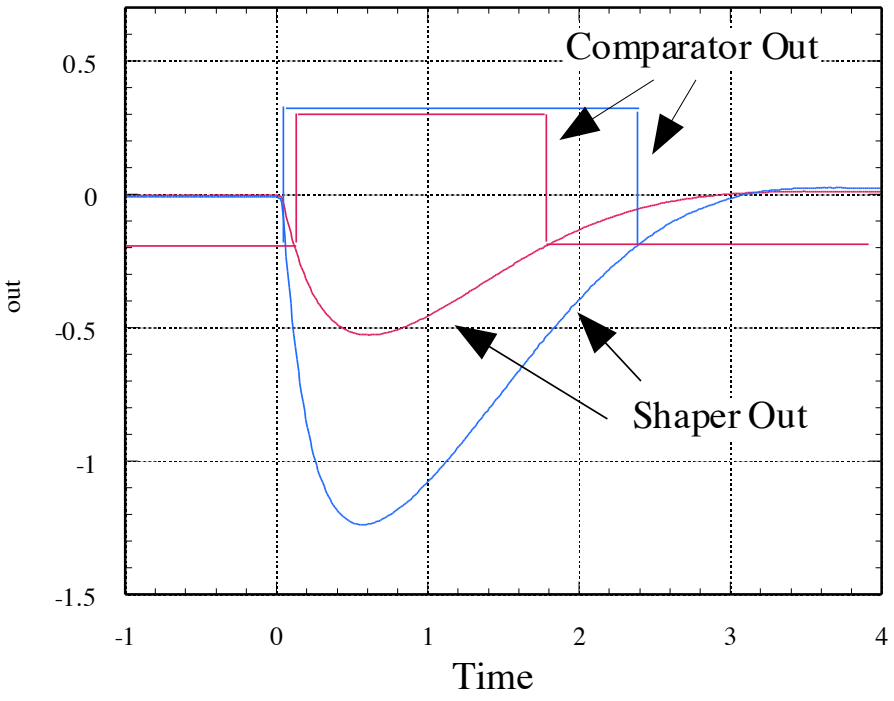


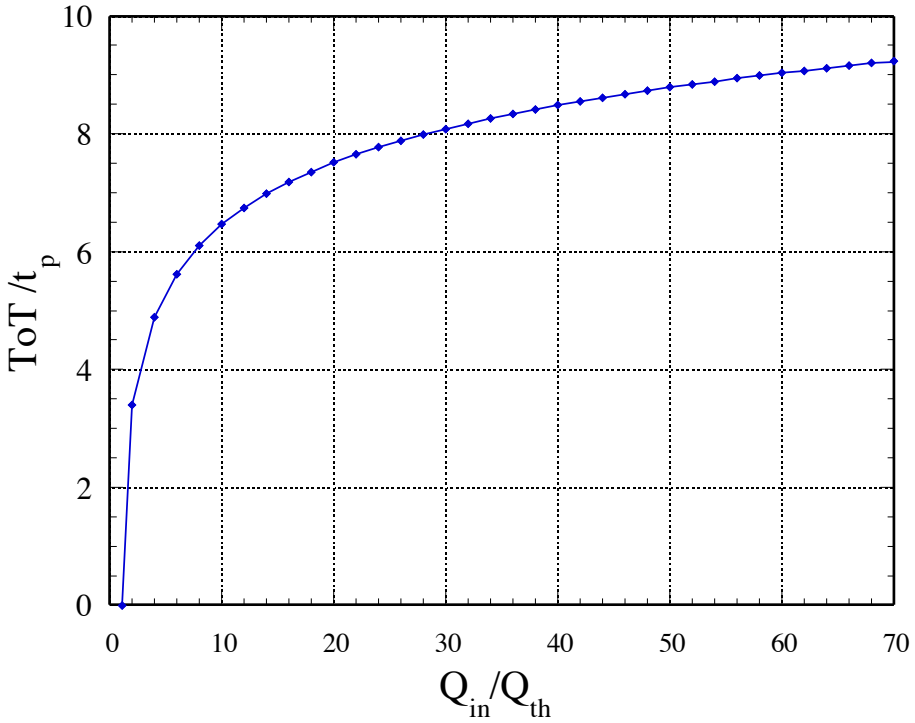
- If the signal at the shaper output returns to the baseline with a constant slope, then a linear relationship exists between the peak amplitude at the shaper output and the ToT duration (the rise time of the shaper output signal is assumed to be negligible)

$$ToT = \frac{V_{peak} - V_{th}}{\left| \frac{dV_{shaper}}{dt} \right|}$$

Range compression with ToT

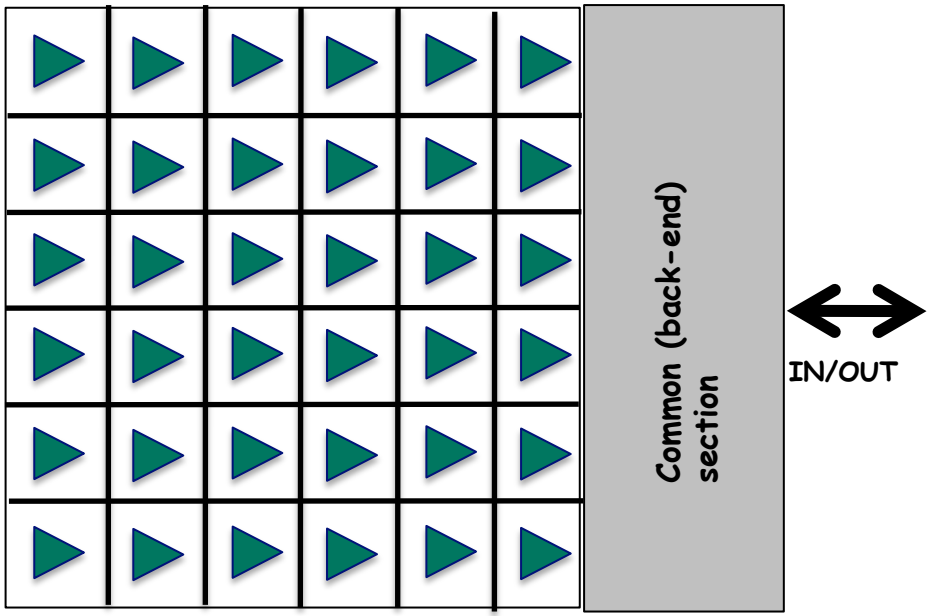
- In the case of linear (constant shape) filtering, the peak voltage-to-ToT duration relationship becomes a non linear one; in particular, a compression of the characteristic may be achieved in such a way that both high resolution at small input charge and high dynamic range can be obtained





General features of readout chips

- A readout chip for semiconductor detectors includes both analog and digital blocks; it contains a section where a cell is periodically replicated based on the detector chip geometry, and a common (completely digital) section servicing all the cells
- The analog front-end performs the task of amplifying and suitably shaping the charge signal in order to maximize the signal to noise ratio
- Digital blocks may perform several tasks, like data selection (sparsification), zero suppression, hit counting, analog-to-digital conversion, time stamping, data storing, buffering and serialization (or parallelization)

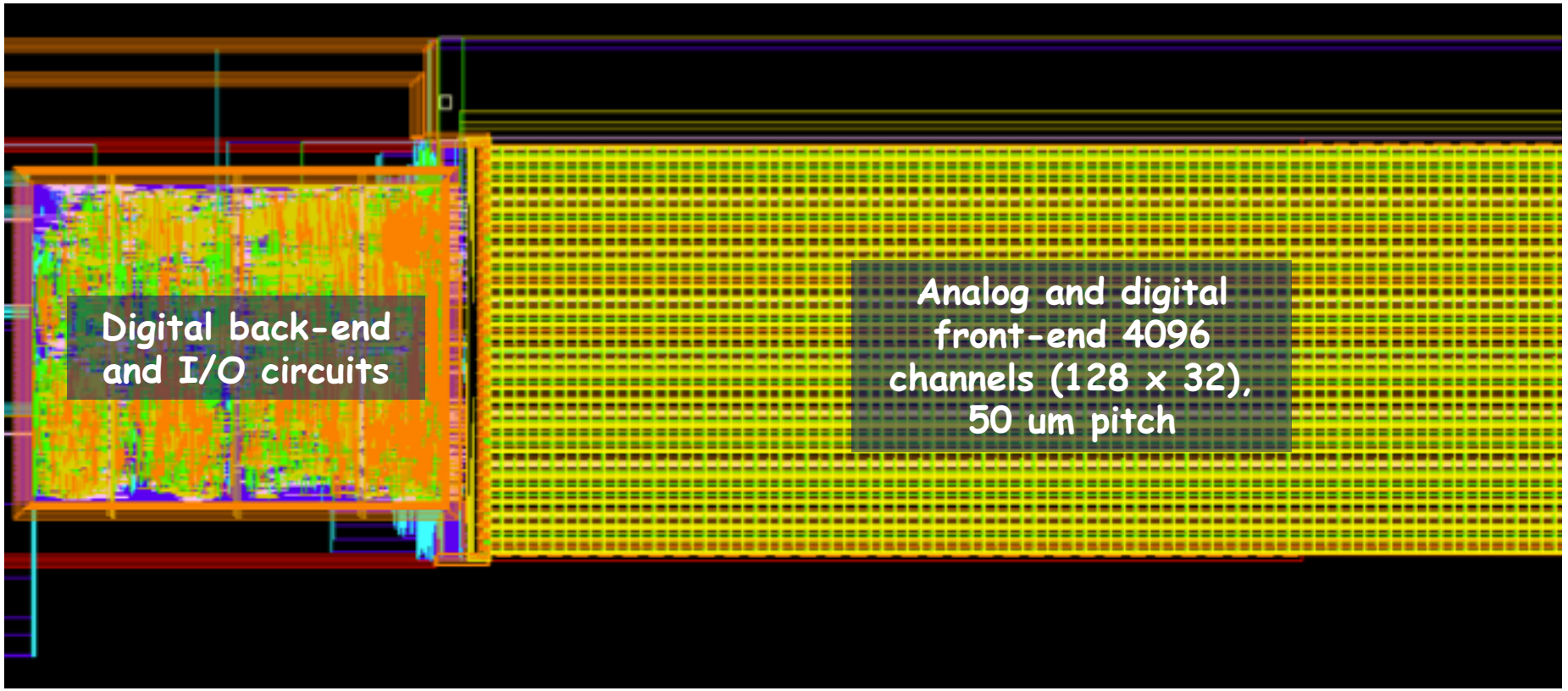


Front-end section (one cell for-each sensor element)

- A readout chip has to provide digital information in a form that requires the least readout bandwidth and processing time possible before being stored in a disk; therefore, as many functions as possible are moved from the acquisition system to the chip itself

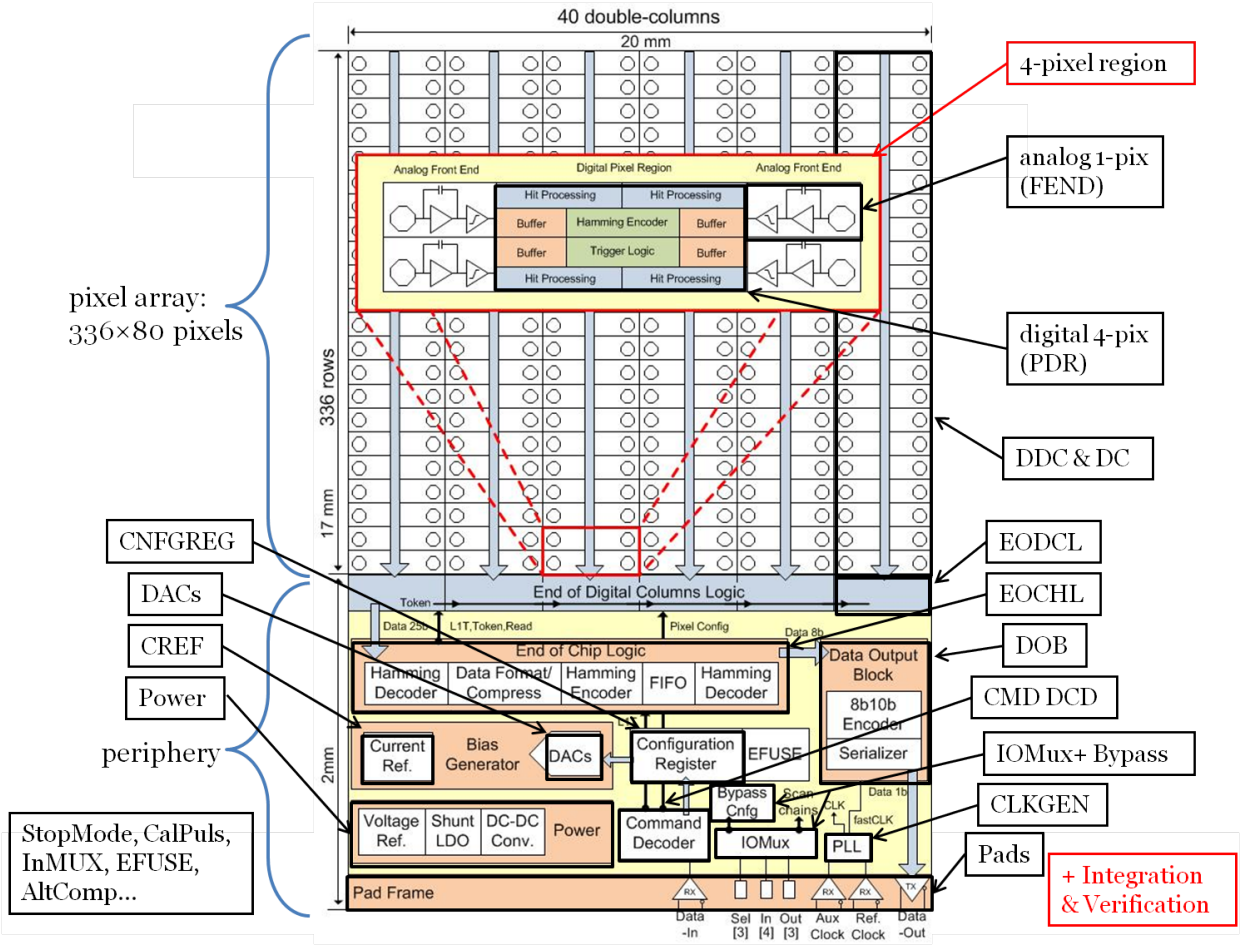
SuperPix0 chip for hybrid pixel detectors

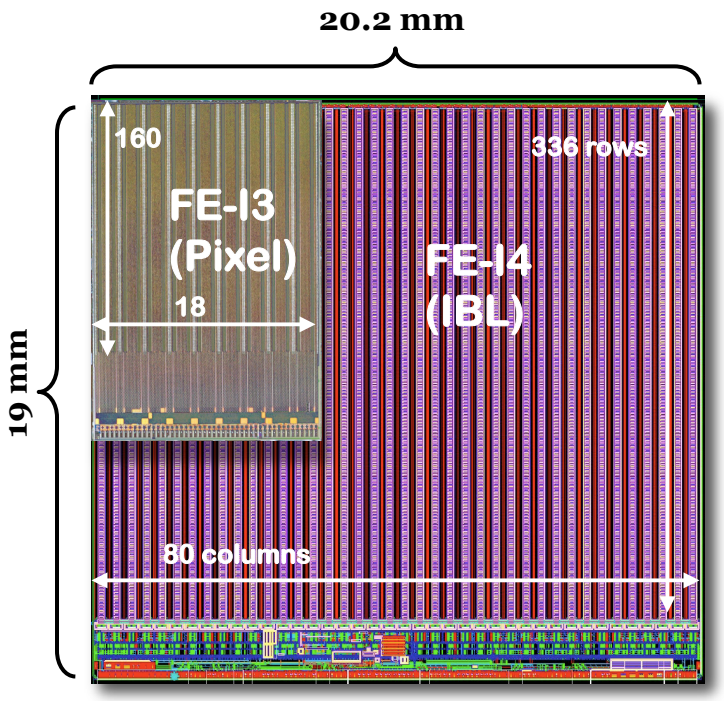
- Fabricated in a 130 nm CMOS technology – mixed signal chip for hybrid pixel
- Sparsified readout based on a macropixel structure



FE-I4 chip for the ATLAS IBL

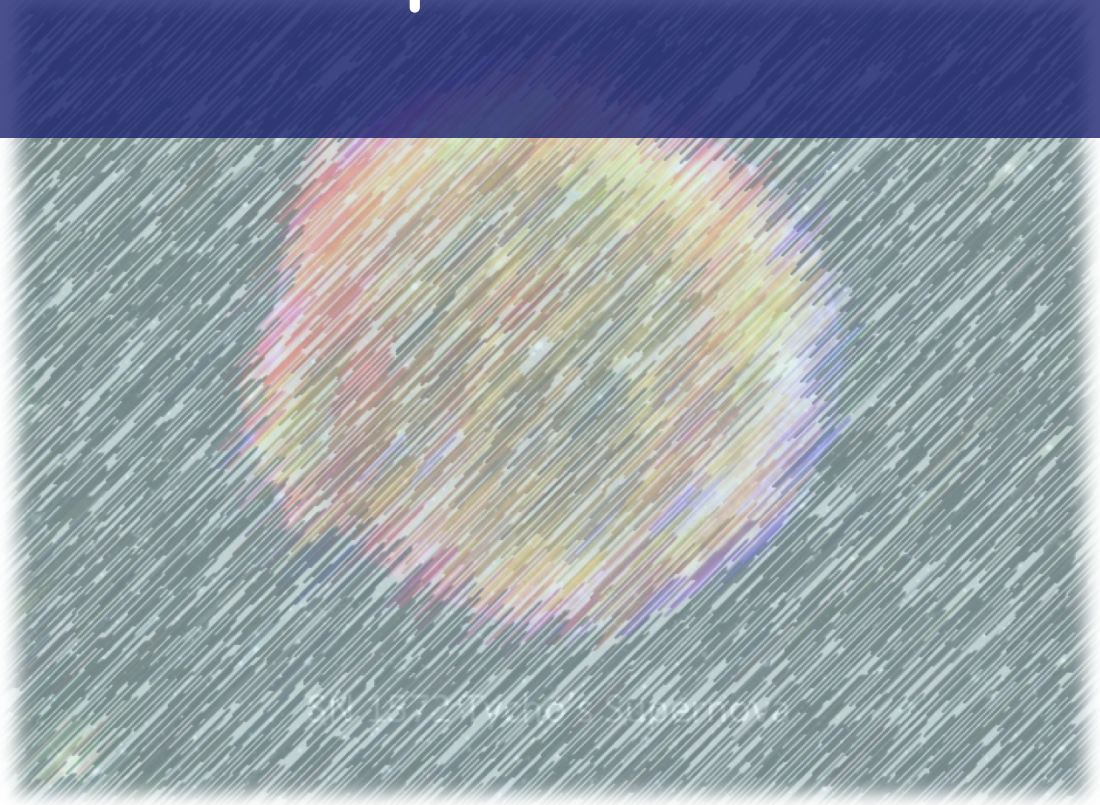
- CMOS 130 nm mixed-signal chip





- Power regulation
- Command decoding and trigger management
- Internal signal monitoring and diagnostic recording and reporting
- Data formatting and high speed serialized output, including clock generation

Enabling technologies for advanced pixel detectors

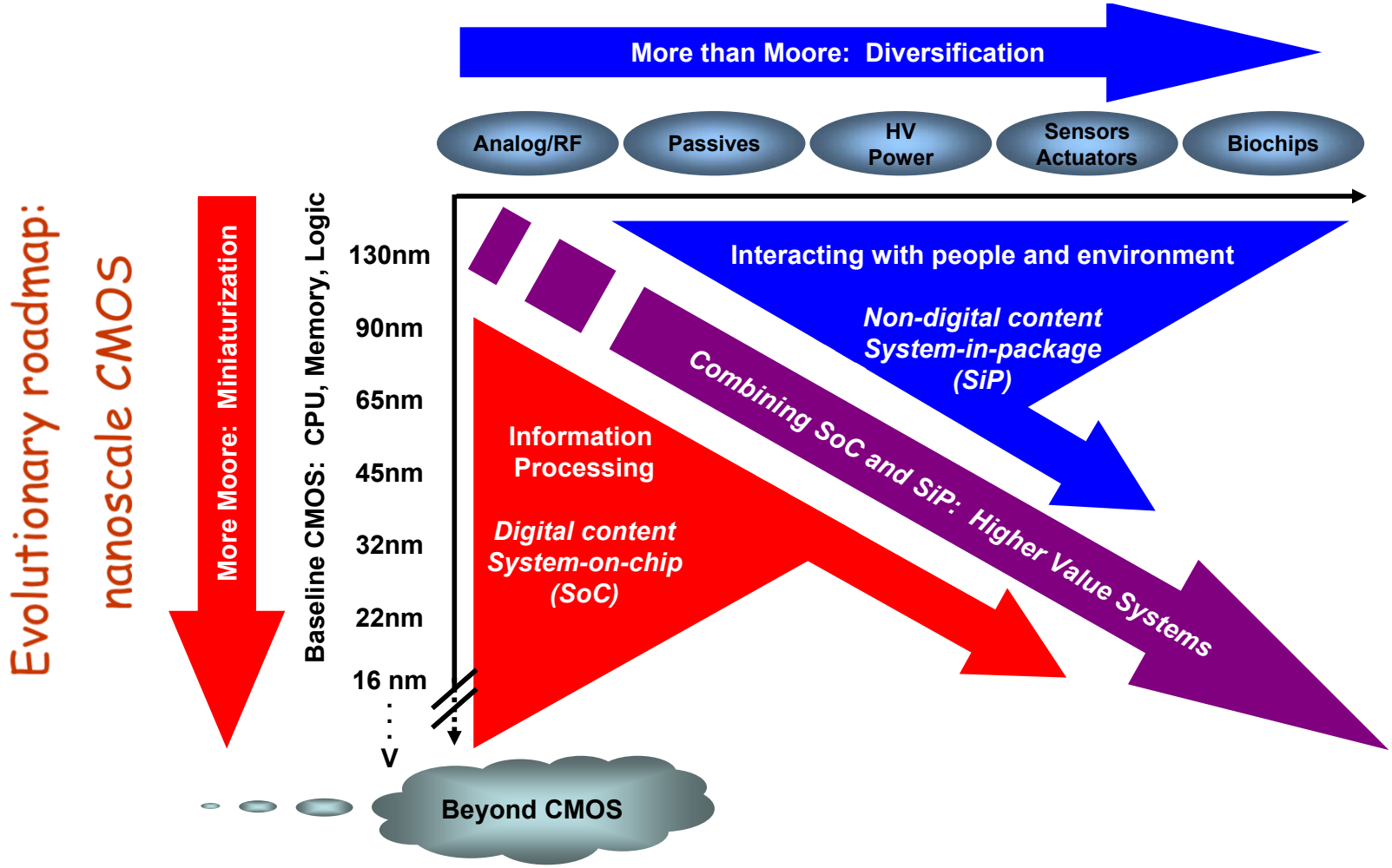


Nanoscale CMOS and 3D integration

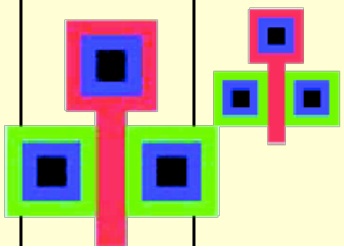
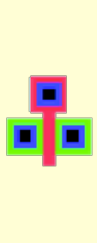
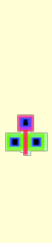
- New applications of semiconductor detectors in high energy physics (silicon vertex trackers) and photon science (high-resolution imagers) set demanding and often conflicting requirements on the front-end electronics
  - more electronic intelligence squeezed in smaller pixel cells
  - larger amount of data stored in the chips and then transmitted outside
  - lower power
  - tolerance to higher radiation levels
  - minimum amount of material and dead areas
- The potential of current microelectronic processes (including interconnections) has to be exploited, in particular
  - standard, nanoscale CMOS technology
  - vertical integration technology

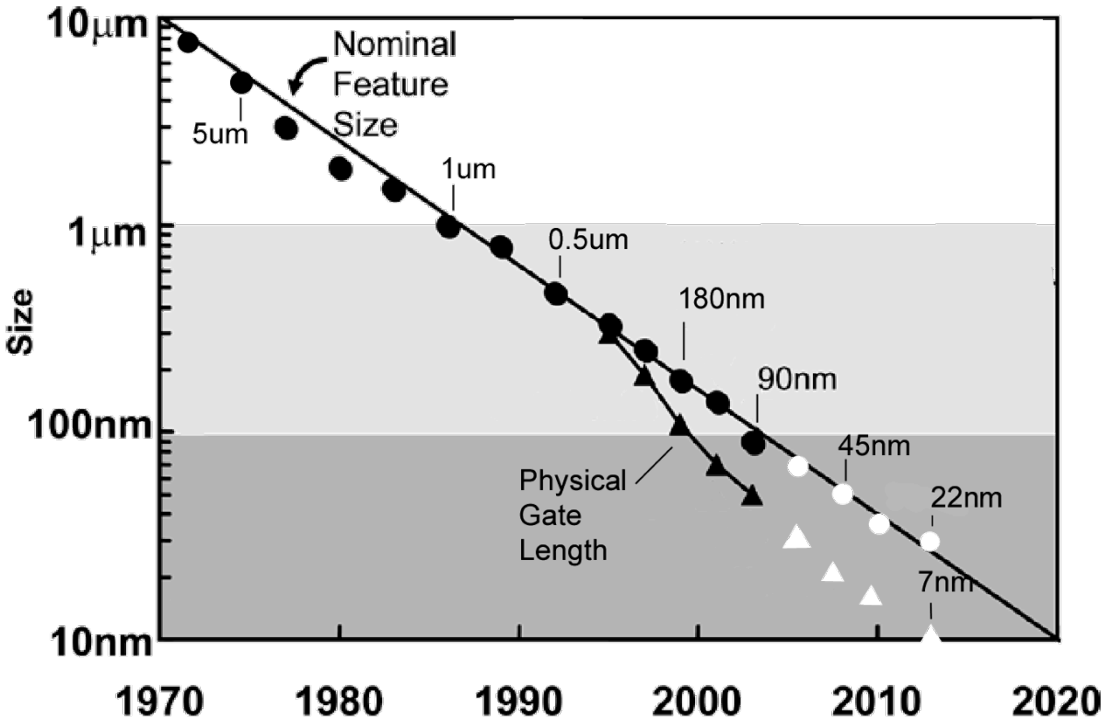
Evolution of microelectronic technology

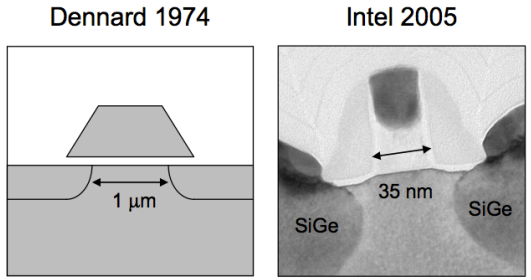
No roadmap, room for new ideas: monolithic sensors, 3D integration



Industry scaling roadmap for CMOS

Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										



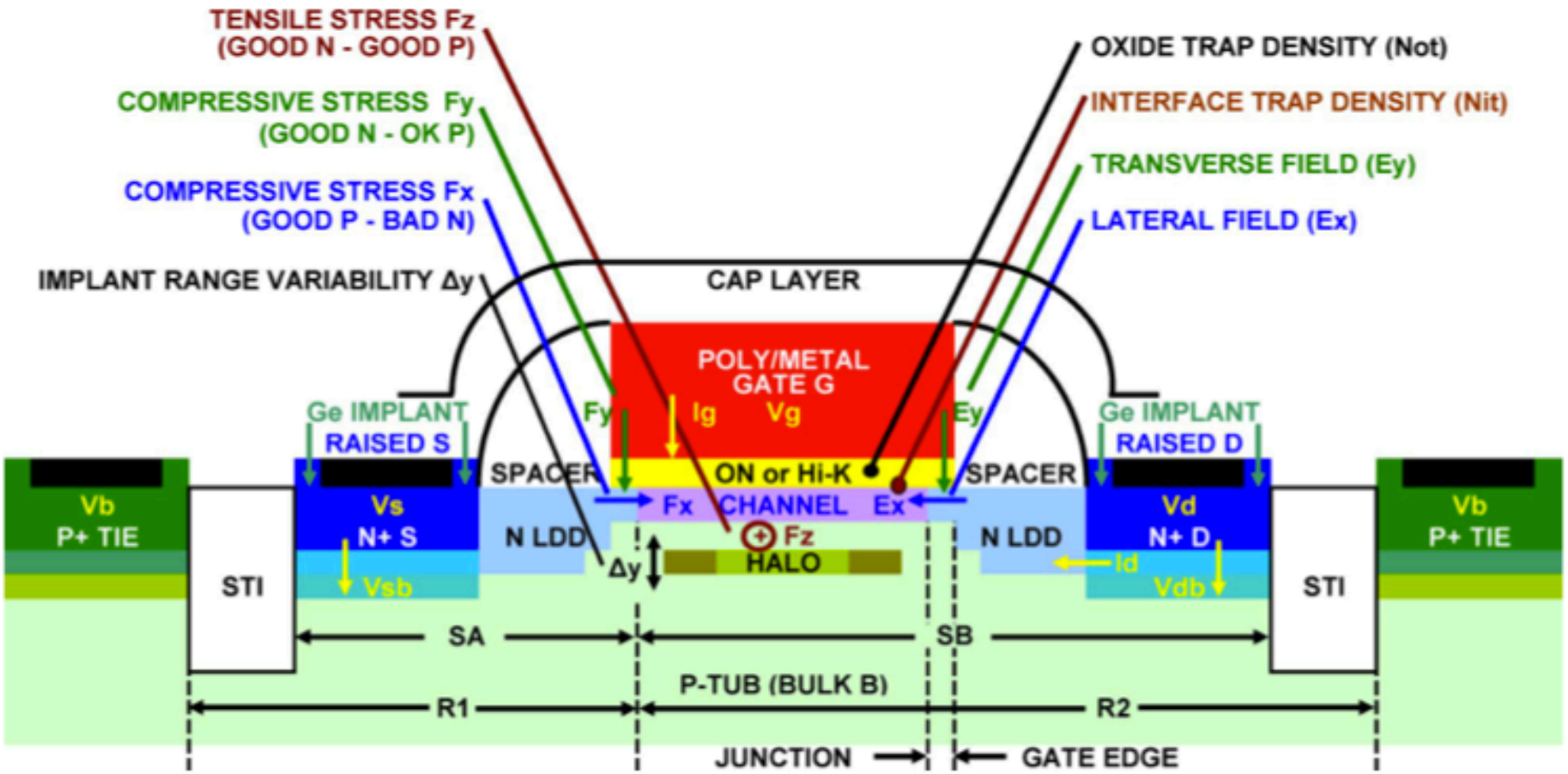


	Dennard 1974	Intel 2005
Gate Length:	1.0 µm	35 nm
Gate Oxide Thickness:	35 nm	1.2 nm
Operating Voltage:	4.0 V	1.2 V

Classical scaling ended in the early 2000s due to gate oxide leakage limits

Bohr, "the new Era of Scaling in a SoC world", 2009 ISSC

Nanoscale MOSFET devices

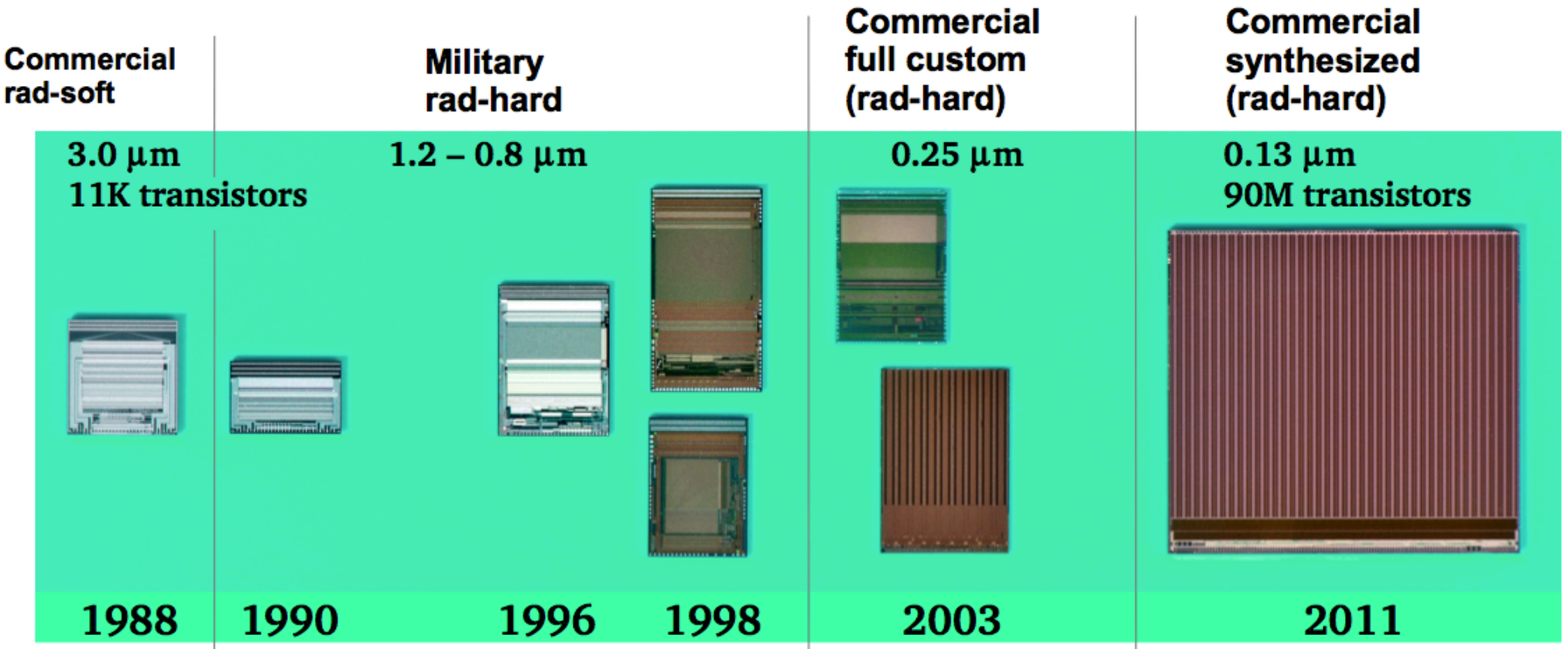


Lewyn et al, "Analog circuit design in nanoscale CMOS technologies", Proc. IEEE, Vol. 97, no. 10, Oct. 2009.

Reasons for CMOS scaling

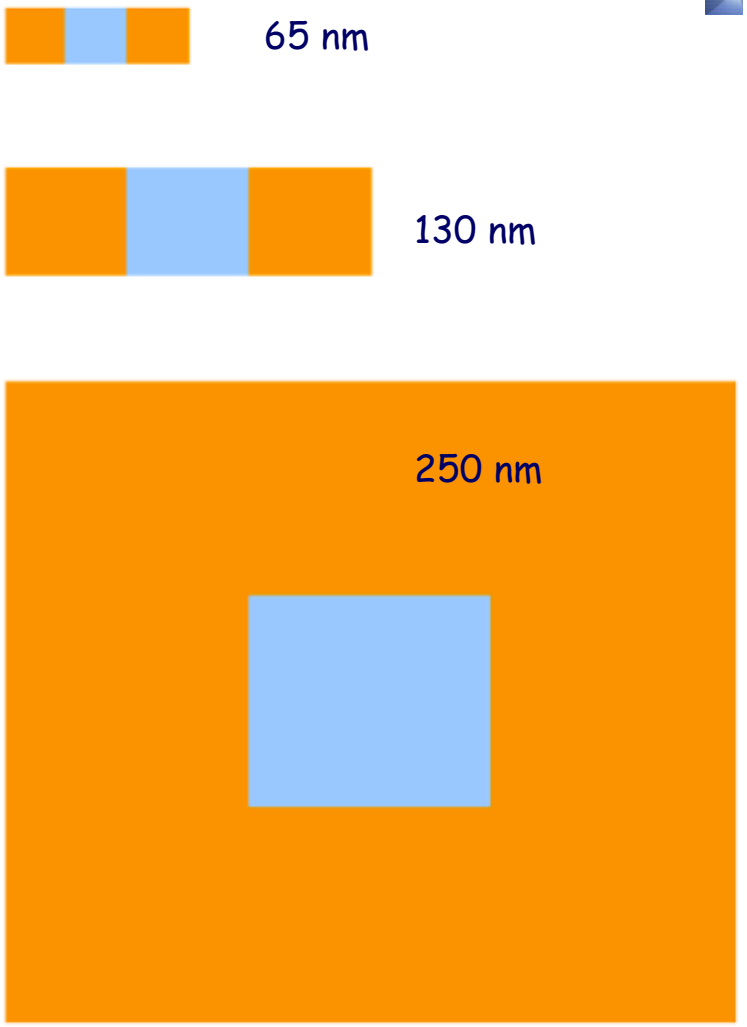
- Industrial microelectronic technologies are today well beyond the 100 nm frontier, bringing CMOS into the nanoscale era
- Digital performance (speed, density, power dissipation) are driving the evolution of CMOS technologies towards a continuous shrinking of physical feature sizes
- **Analog performance** remains essential for the processing of signals delivered by semiconductor detectors
- Front-end electronics may benefit from scaling in terms of functional density (small pitch pixels) and digital performance - analog design is a challenge (reduced supply voltage and dynamic range, statistical doping effects, …)
- For a full integration of analog and digital circuits in the most modern semiconductor technologies, design advances are needed to exploit the full potential: digital signal processing may be used to overcome analog limitations, analog circuits may be used to monitor the performance of digital circuits and their power consumption

Chips for vertex detectors at colliders

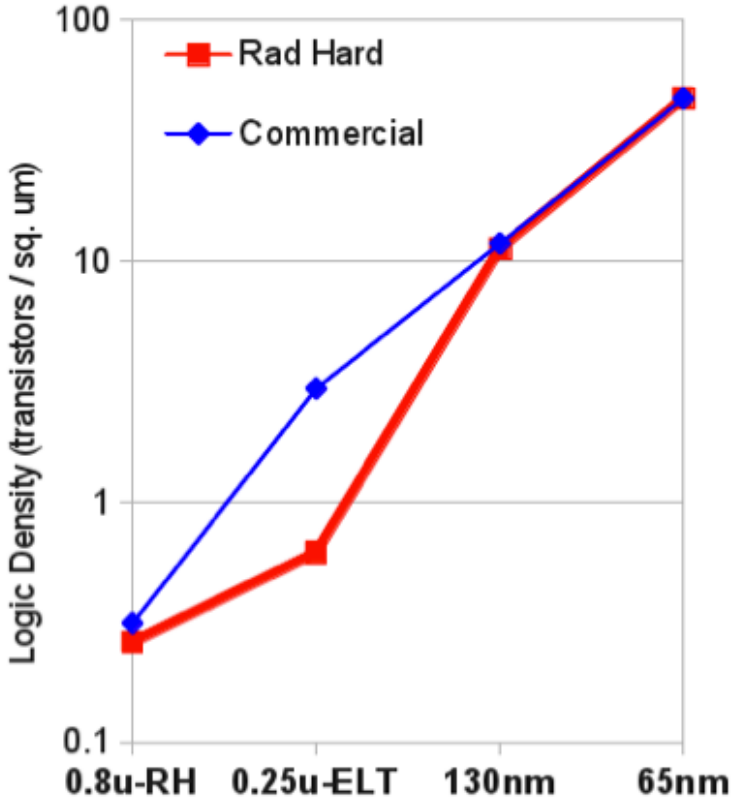


M. Garcia-Sciverez, "Towards the Next Generation of Pixel Readout Chips", Pixel 2012 Conference

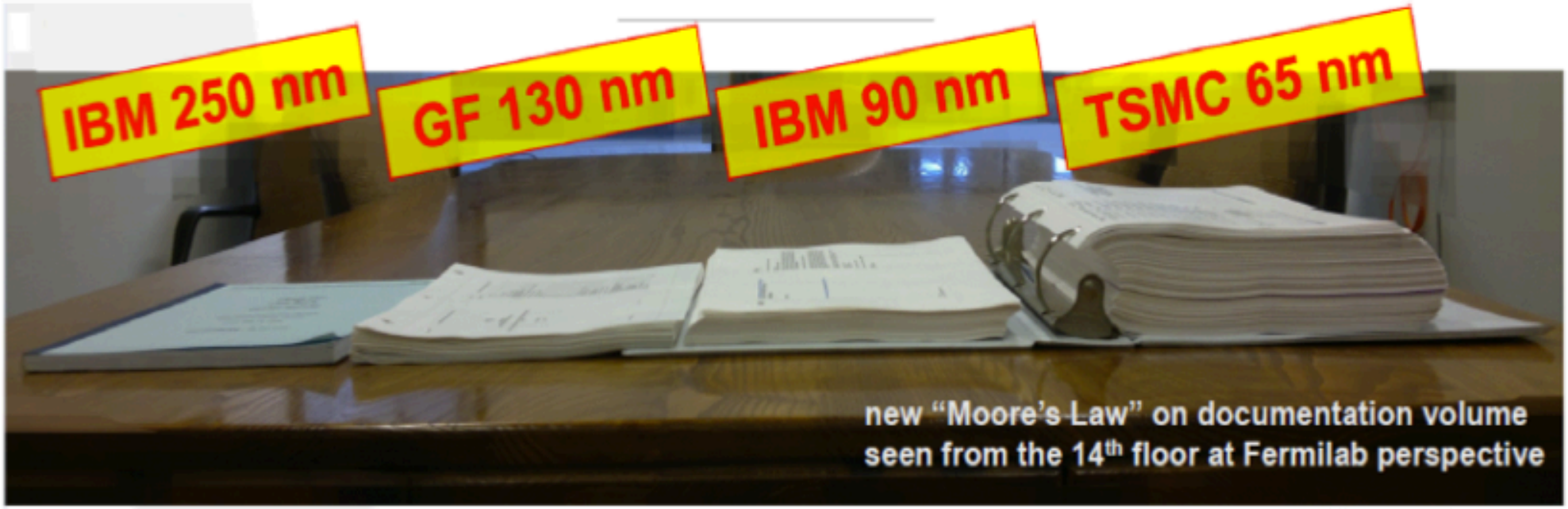
Rad-hard logic in detector front-end chips



- Logic circuits in radiation detectors front-end chips lagged Moore's law due to the need for enclosed layout transistors (ELT), but are now catching up



Moore's law for DRMs



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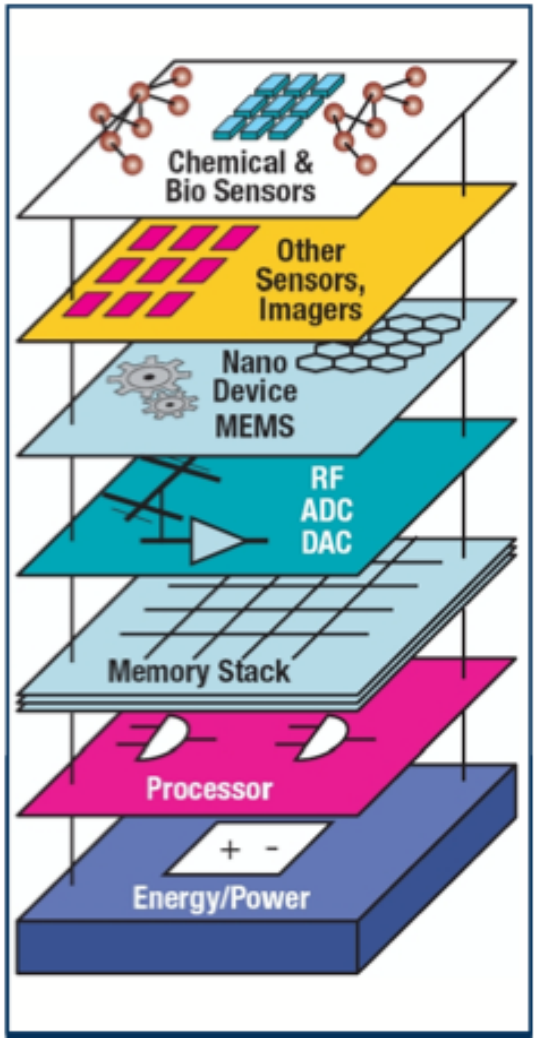
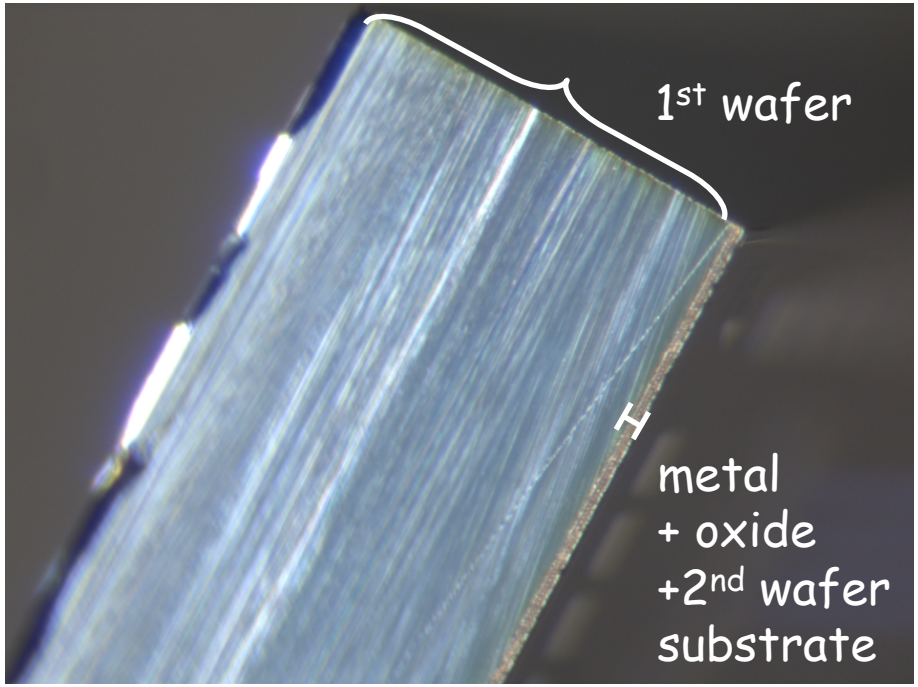
3D integration of microelectronic circuits and sensors



- 3D integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together
- Intense research activity ongoing in academia and industry: MIT Lincoln Labs, IBM, INTEL, SEMATECH, Tezzaron in the US, CEA-LETI, Fraunhofer Institute and IMEC in Europe, T-Micro in Japan
- Presently pursued applications
  - vertically integrated, high resolution CMOS imagers
  - 3D stacked flash memories
  - 3D integration of processor and memory subsystems

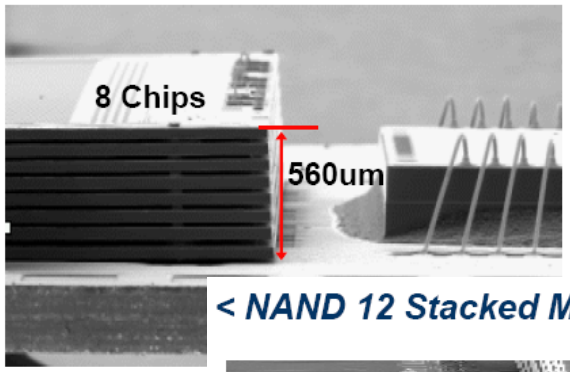
J.-Q. Lu, K. Rose, and S. Vitkavage, "3D Integration: Why, what, who, when?," Future Fab Int., no. 23, pp. 25–27, 2007.

Vertical integration process



< 2 layer MAPS for particle tracking >

< NAND 8 Stacked Memory Card >



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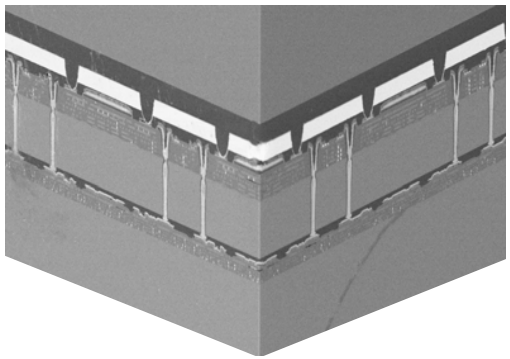
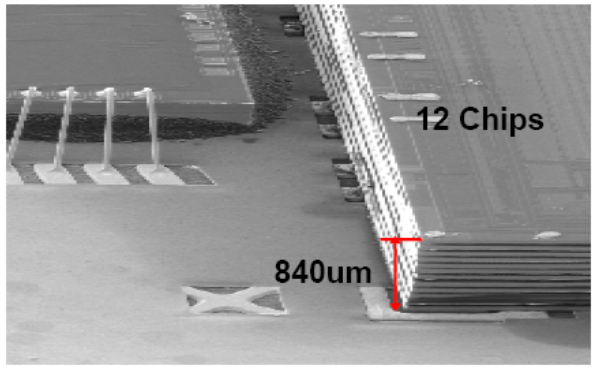
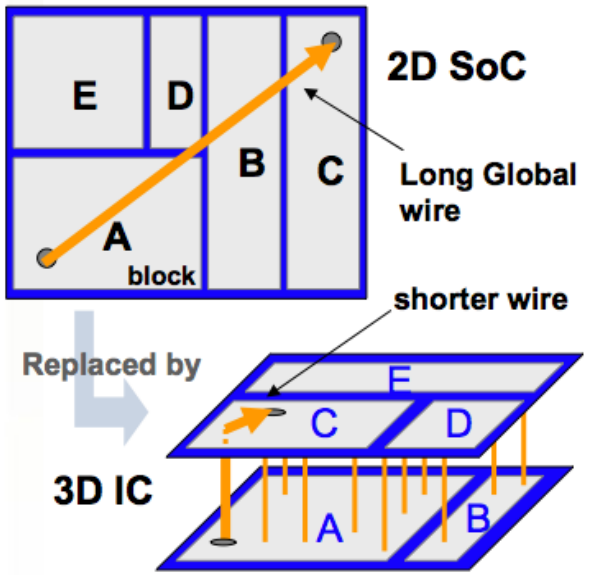




Advantages of 3D integration

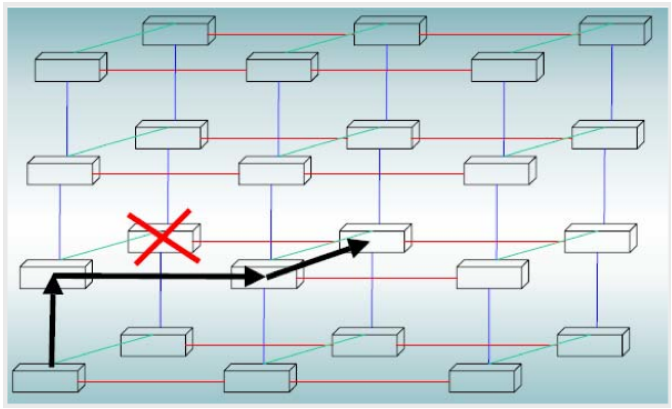


- Replace long horizontal with short vertical interconnects, addressing
  - power dissipation (more than 50% of dynamic power consumption is due to interconnects in modern processes)
  - RC delay (increasing exponentially from technology node to node)
  - crosstalk (more of an issue in mixed signal circuits)
  - form factor

$$P_{dyn} = C\ V^2_{DD}\ f$$

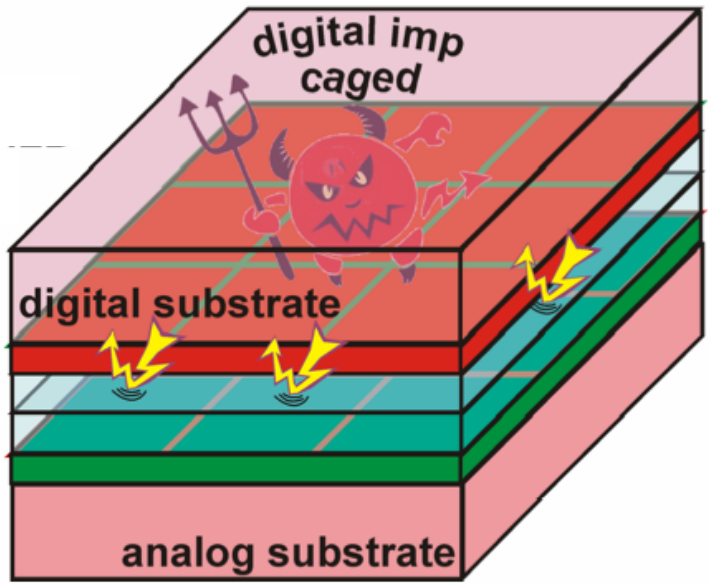
switching capacitance (diffusion, gate, interconnects)

- Enable the integration of heterogeneous devices and technologies (memory, logic, RF, analog, sensors,…)
  - cost reduction (as compared to SoC)
  - new functionalities can be implemented
- Enable higher fault resistance thanks to the high connectivity of 3D ICs

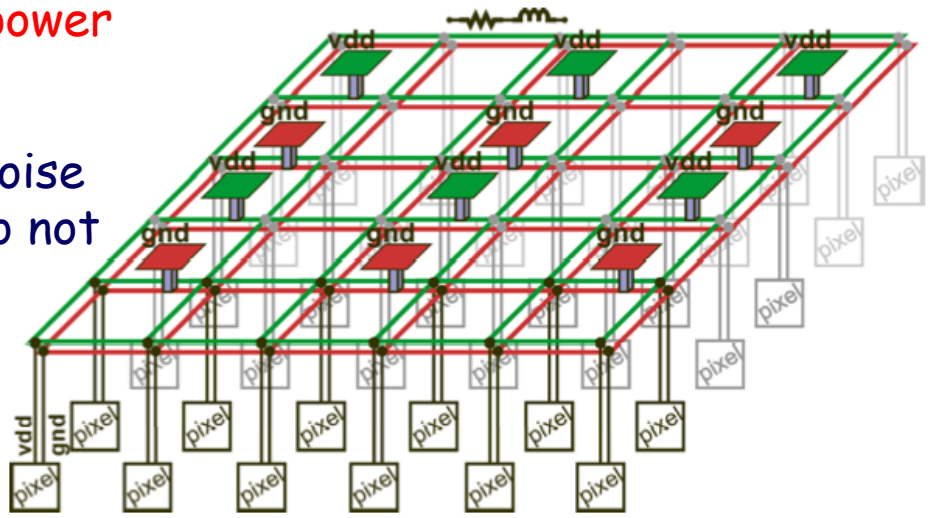


Benefits for pixel detectors

- More efficient and uniform ground and power distribution (against voltage drops)
- Separation of digital activity from low-noise analog part (analog and digital circuits do not share the same substrate)

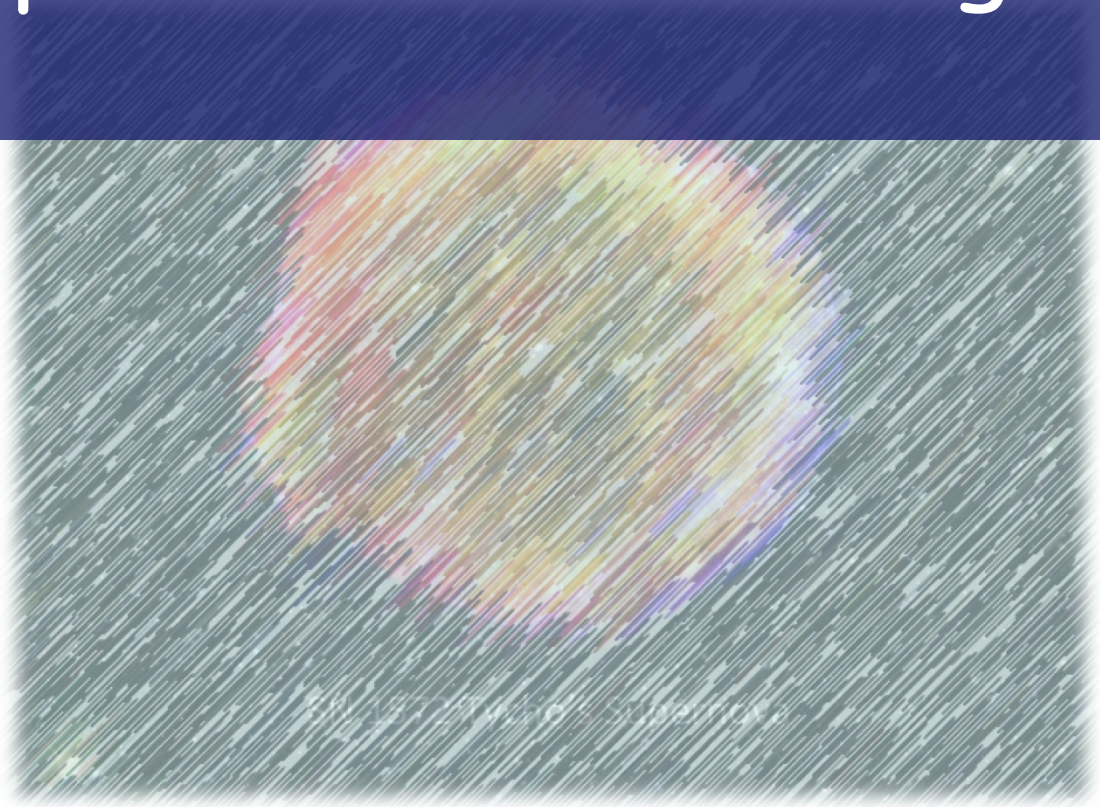


G. Deptuch, "Front-end electronics 4 3D technologies," Vertically Integrated Pixel Sensors Workshop, Pavia, Italy, April 22-24 2010



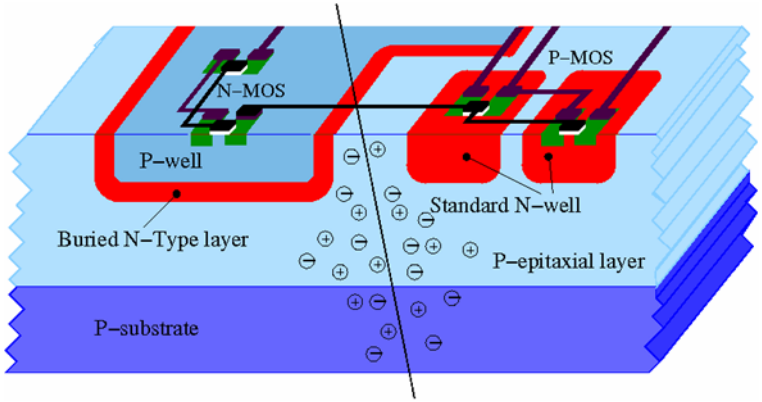
- Post-process thinning (3D wafers obtained by fusion techniques are as rigid as monolithic structures) ➔ less material
- Dead area reduction (readout electronics can be designed with virtually no peripheral circuits ➔ 4-side buttable detectors)

Some examples of advanced pixel detector design

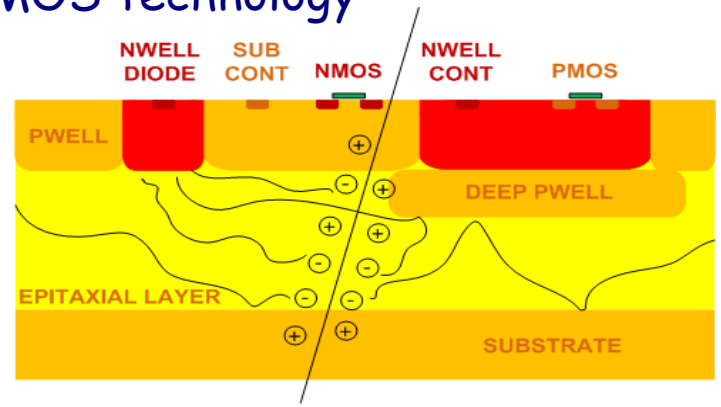


CMOS sensors with hybrid pixel features

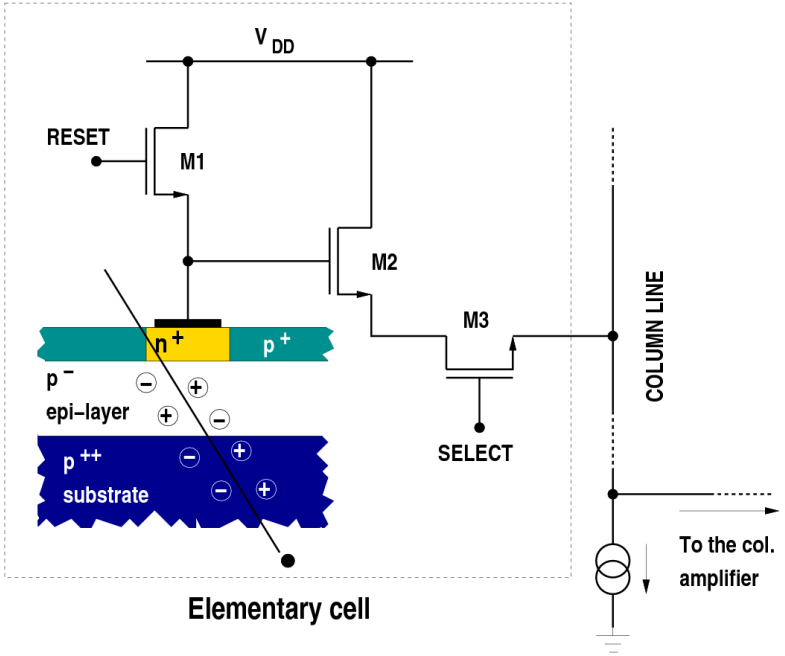
- Some (more or less standard) properties of less scaled CMOS technologies have been exploited to add some new functionalities to monolithic active pixel sensors
  - deep N-well monolithic sensor



  - monolithic sensor in a quadruple well CMOS technology

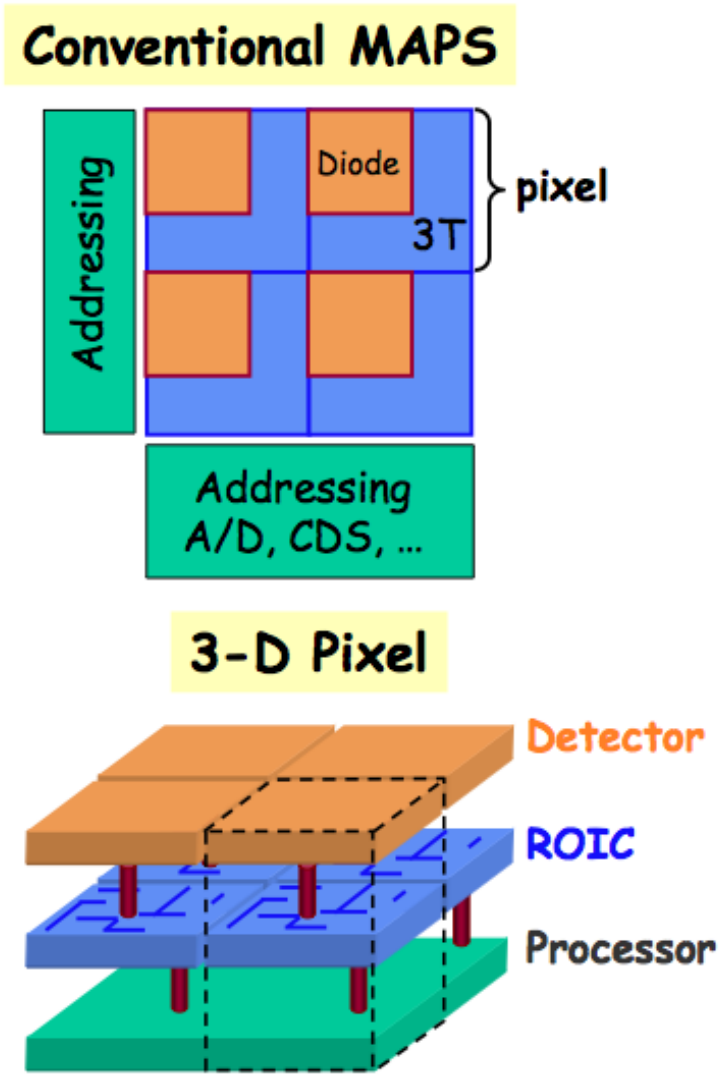


  - standard CMOS MAPS



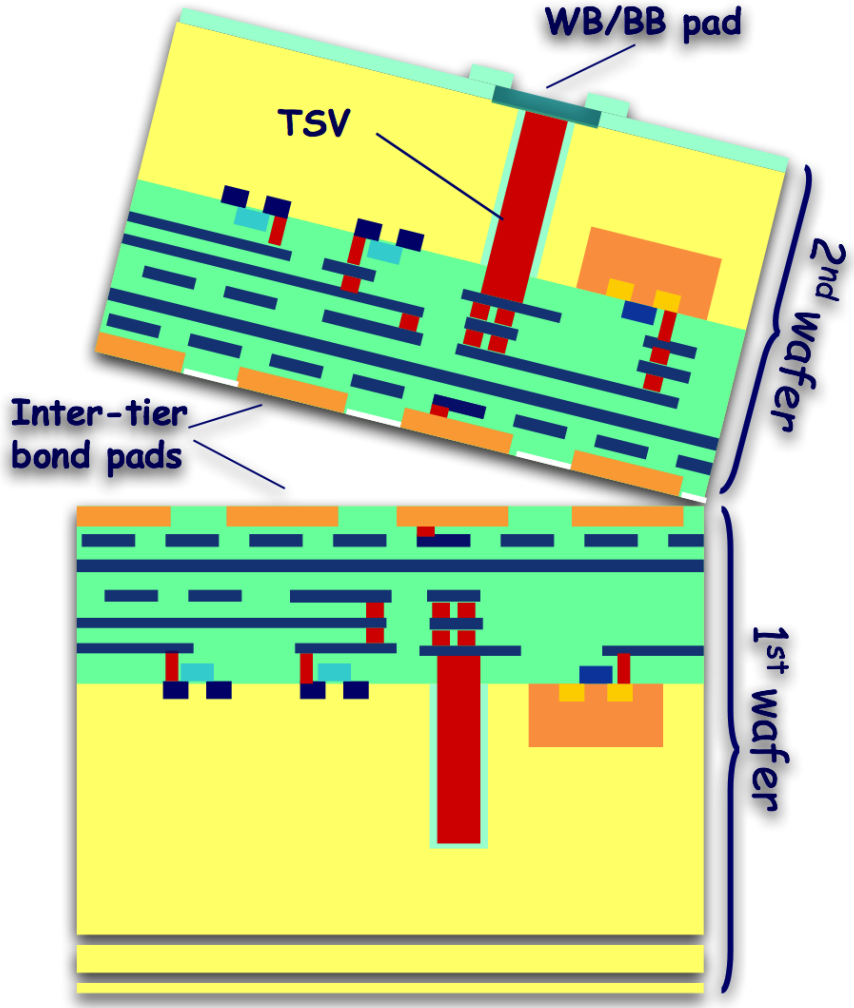
3D pixel sensors

- Vertical integration processes represent a technological leap in the design of monolithic radiation sensors
- In a conventional monolithic sensor
  - the sensor and the front-end electronics share pixel area, with a consequent loss in collection efficiency and/or fill factor; for the front-end electronics and sensor to coexist in the pixel, non optimized design solutions for both have to be accepted
  - control and support electronics is placed outside the imaging area, where they form a dead region for the sensor
- In the 3D version of a monolithic pixel sensor
  - the sensor area can be fully active, resulting in a four-side buttable chip;
  - circuit density and functionality is increased due to the availability of multiple layers of electronics
  - each layer of the detector can be optimized from the standpoint of the fabrication process



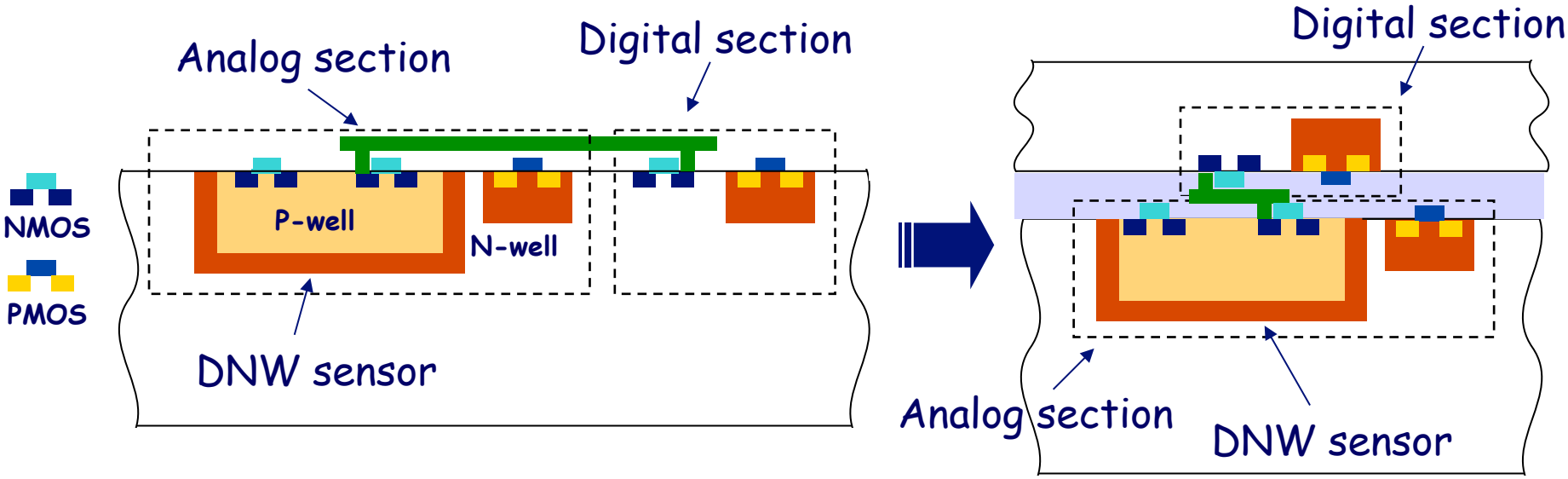
Tezzaron/Chartered homogeneous 3D integration

- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon a set of enabling steps
  - TSV formation
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/ electrical bonding
- Tezzaron Semiconductor technology (via middle approach) can be used to vertically integrate two layers specifically processed by Chartered, now Globalfoundries (130 nm CMOS, 1 poly, 6 metal layers, 2 top metals, dual gate option, N- and PMOS available with different V_{th})



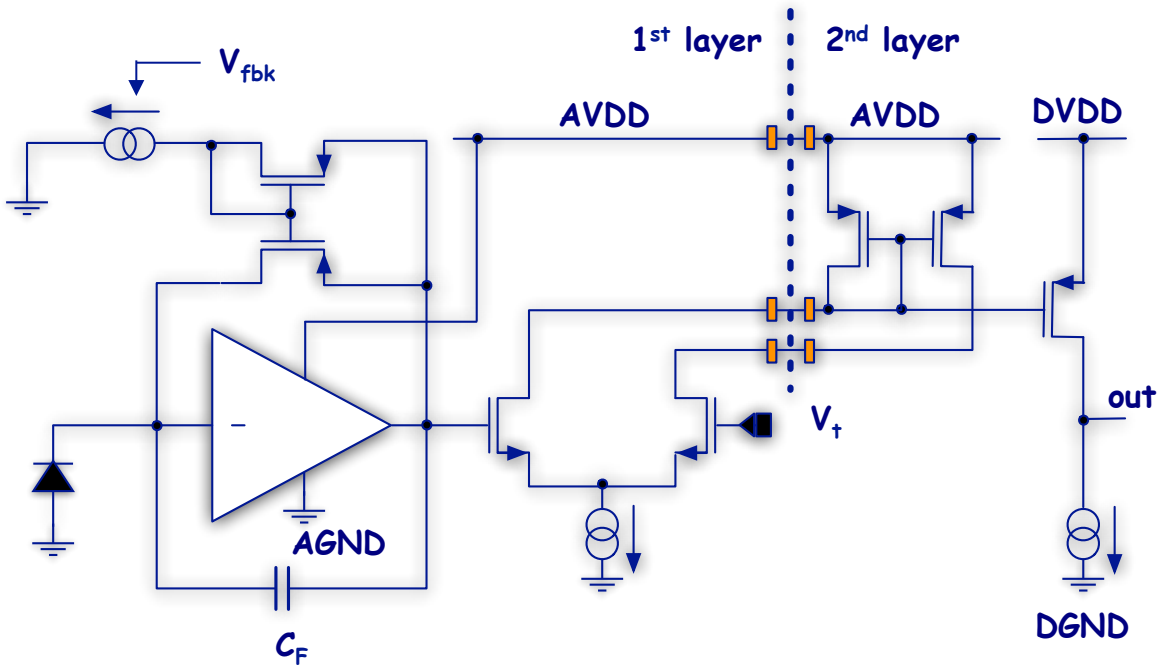
Migration of a 2D DNW MAPS to a 3D process

- Use of a 3D process makes it possible to separate the analog from the digital section to minimize cross-talk between digital blocks and sensor/analog circuits

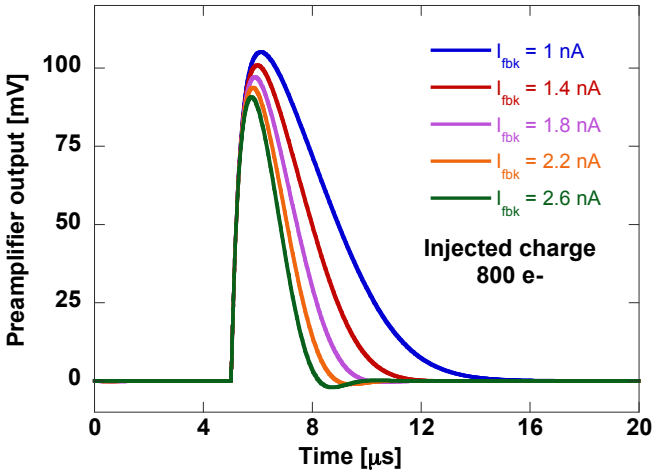


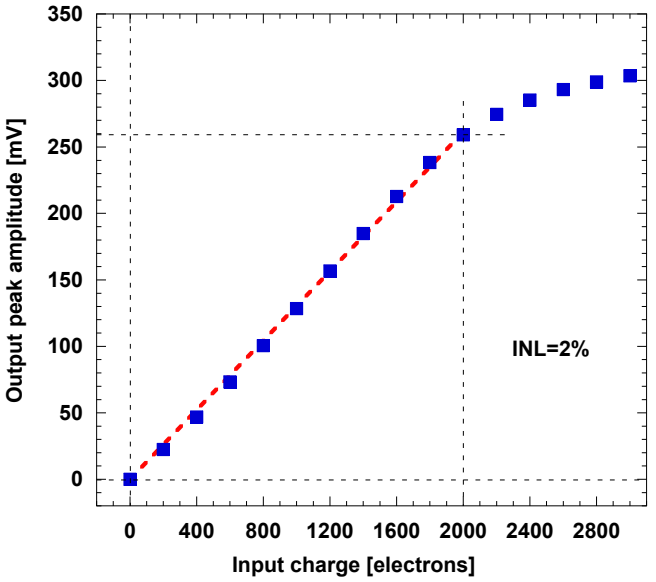
- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Analog FE and discriminator for a 3D MAPS

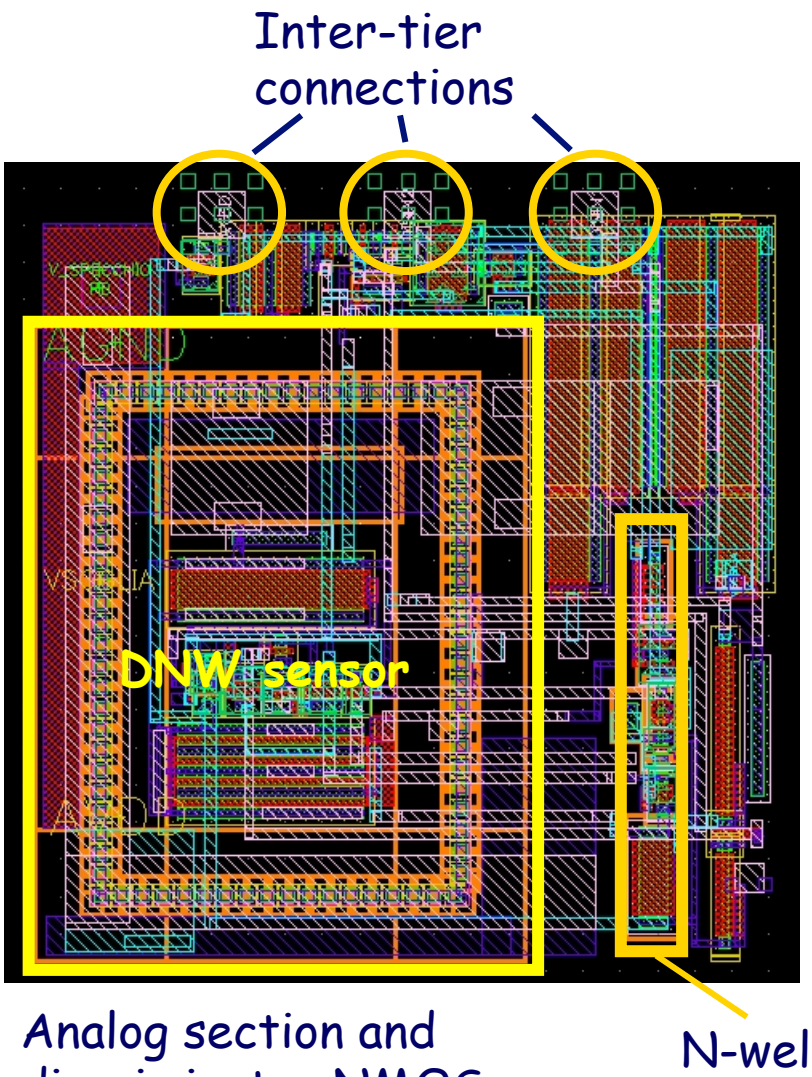


- 20 µm pitch
- W/L=20/0.18
- I_D=1.4 µA, power dissipation=5 µW
- C_D=200 fF
- ~1 µs peaking time
- Power cycling capabilities
- Charge sensitivity (G_Q): 800 mV/fC
- Equivalent noise charge (ENC): 35 e-
- Threshold dispersion (ΔQ_t): 36 e- (28 e- from the SFE, 22 e- from the discriminator)

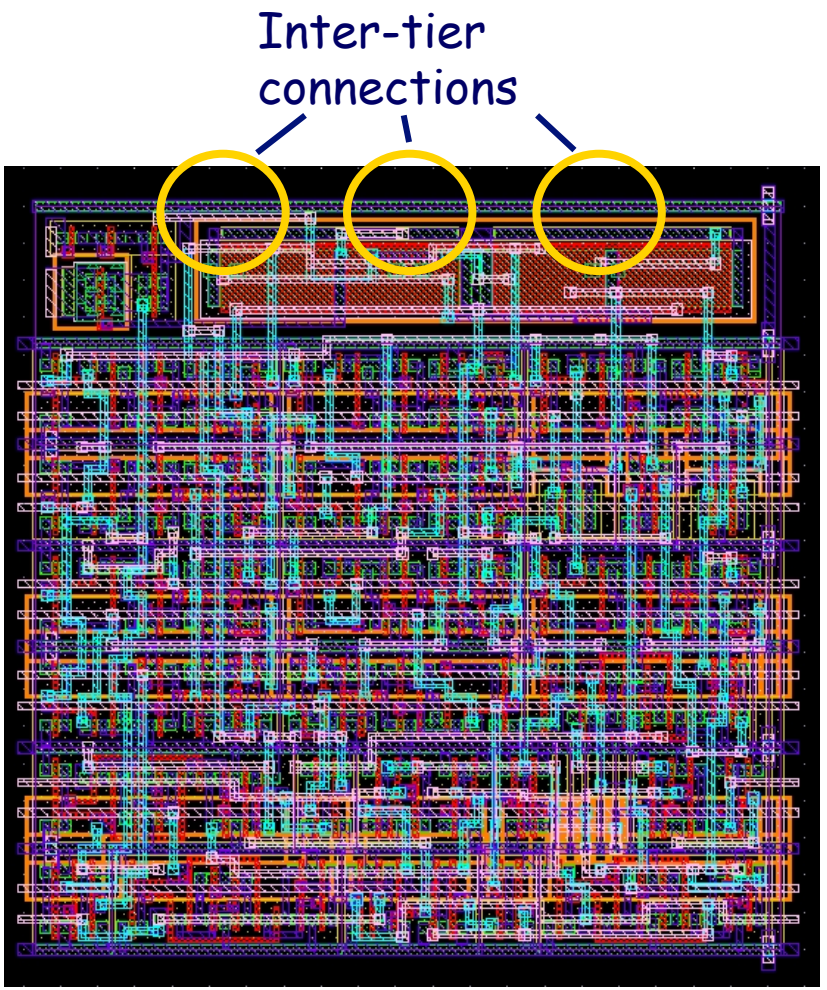




Elementary cell layout: bottom and top tiers



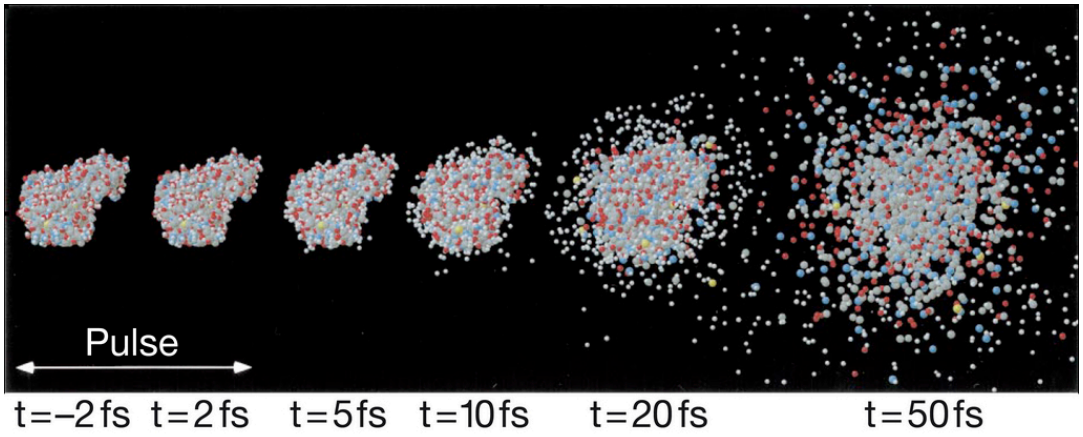
Analog section and discriminator NMOS



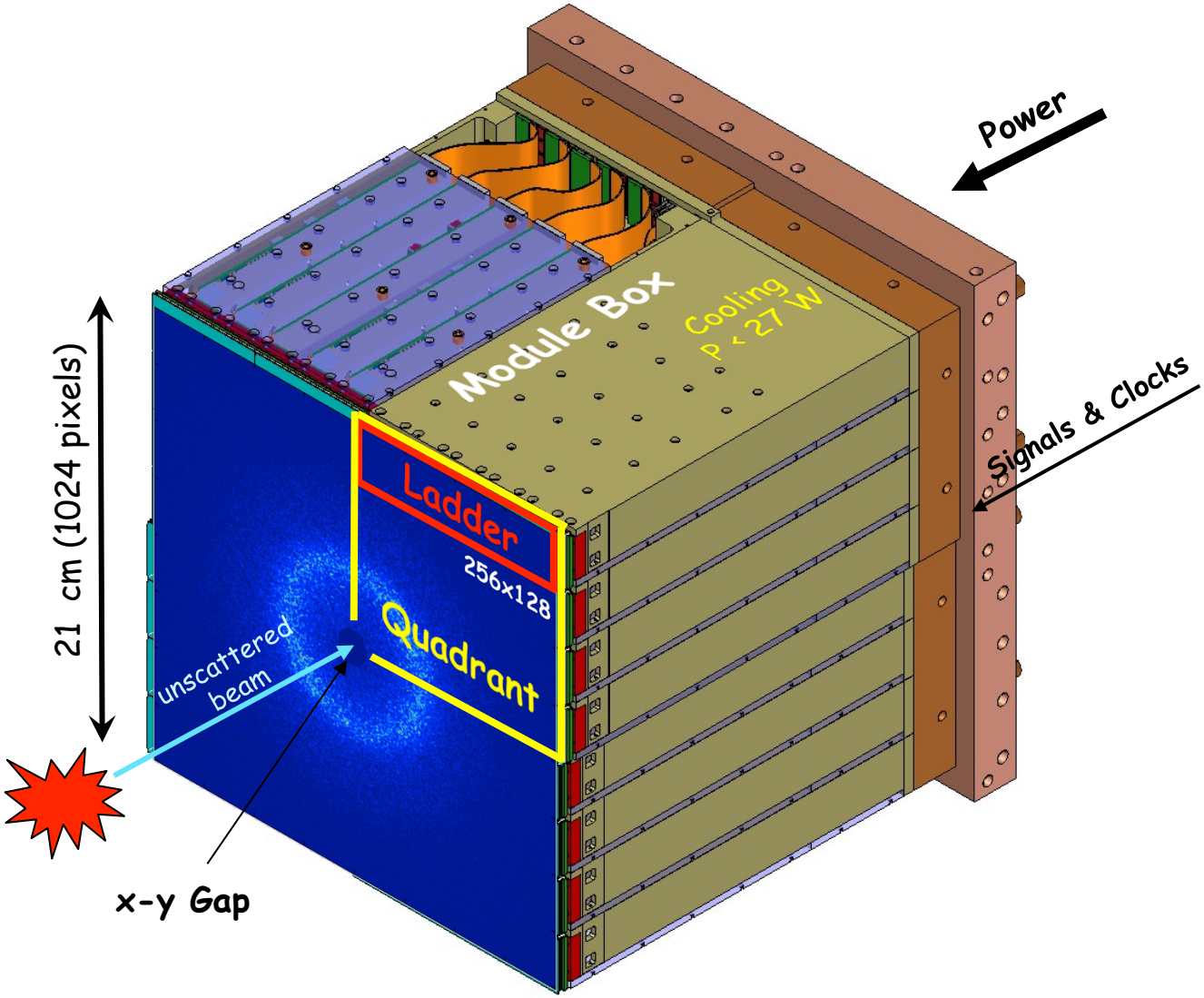
Digital section and discriminator PMOS

Requirements for applications at FELs

- Free electron lasers are bound to become the predominant tool for the investigation of natural phenomena in several fields: structural biology, chemistry, material science, atomic and molecular science
- FELs emit high intensity beams of ultrafast X-rays
  - energy range: 100 eV to 10 keV (λ from 10 nm to 0.1 nm)
  - pulse duration: tens of femtoseconds to picoseconds
  - repetition rate: 100 Hz (continuous mode) to 5 MHz (burst mode)
- A wide dynamic range is foreseen for the signal emerging from the X-ray interaction with the samples under test – 1 to 10000 photons (➔ 80 dB) and single photon sensitivity ➔ severe requirements for the front-end channel noise and sensitivity properties and for the ADC resolution



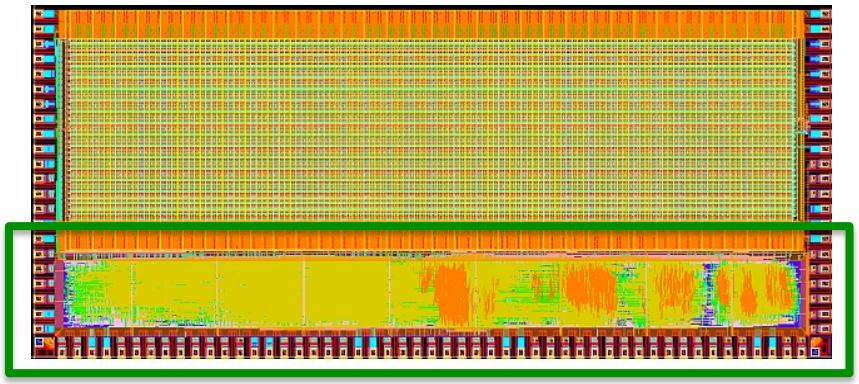
DSSC X-ray camera



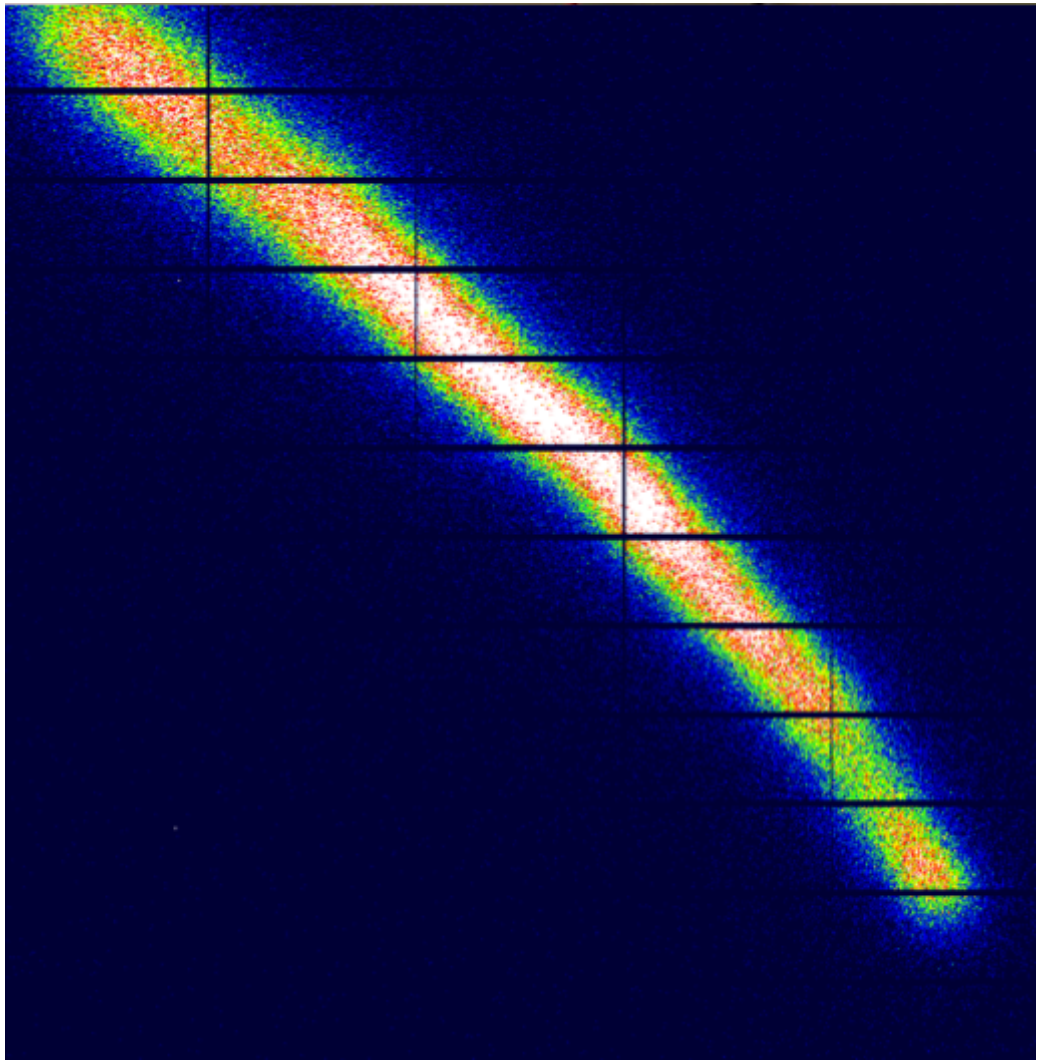
- 1024x 1024 pixels
- 16 ladders/hybrid boards
- 32 monolithic sensors 128x256 6.3x3 cm^2
- DEPFET Sensor bump bonded to 8 Readout ASICs (64x64 pixels)
- 2 DEPFET sensors wire bonded to a hybrid board connected to regulator modules
- Dead area: ~15%

Dead area issue in radiation detectors

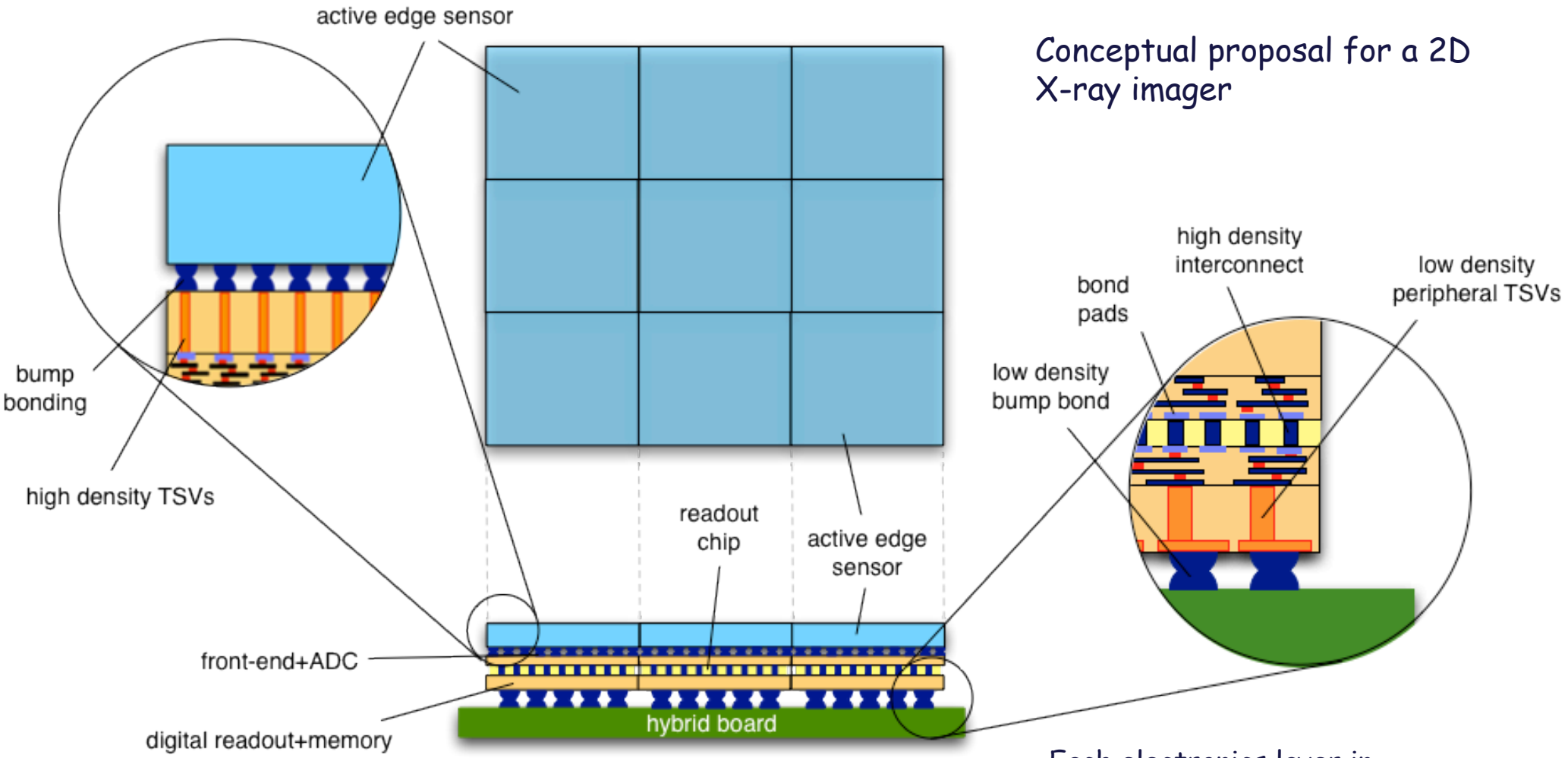
- Modules of limited size
- Gap between modules ➔ missing data



- Dead area generally corresponding to the area taken by the readout circuits at the periphery of the chip
- The sensing layer itself may include some dead area (e.g., guard rings)



Enabling technologies for 4-side buttable modules



Conceptual proposal for a 2D X-ray imager

Each electronics layer in CMOS 65 nm

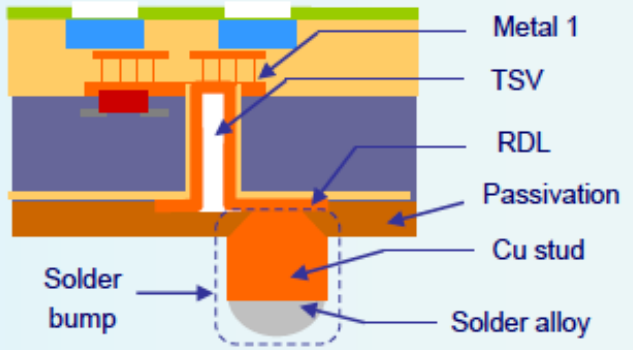
Enabling technologies for a 4-side buttable module

- Low density TSVs for chip to PCB bump-bonding

CEA-LETI

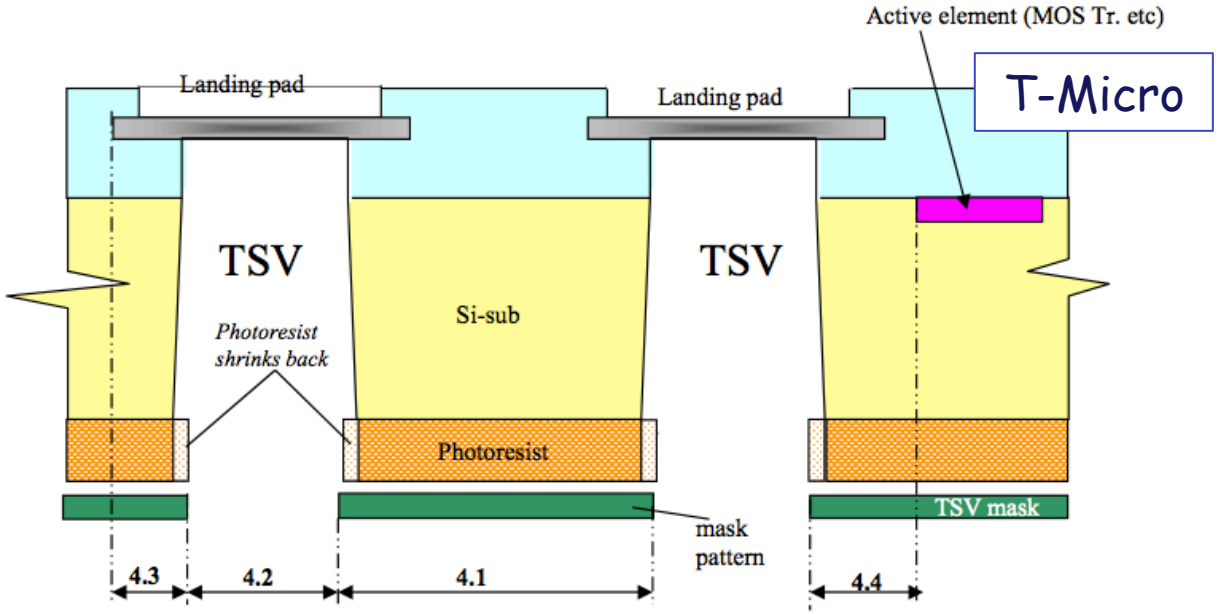
Solder bumps DRM & schematic

- Wafer size : **200 & 300 mm**
- Solder bumps material : **Cu stud / SnAg solder**
- Minimum pitch : **120 µm**
- Solder pillar diameter : **60-80 µm**
- Solder pillar thickness : **Cu 35-40 µm / SnAg 25-30 µm**

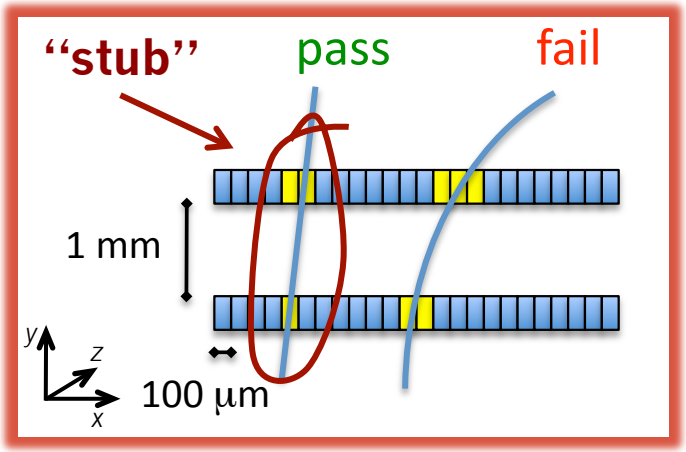


- No gaps, no need for complicate tiling (provided that the detector has minimum dead area)

T-Micro

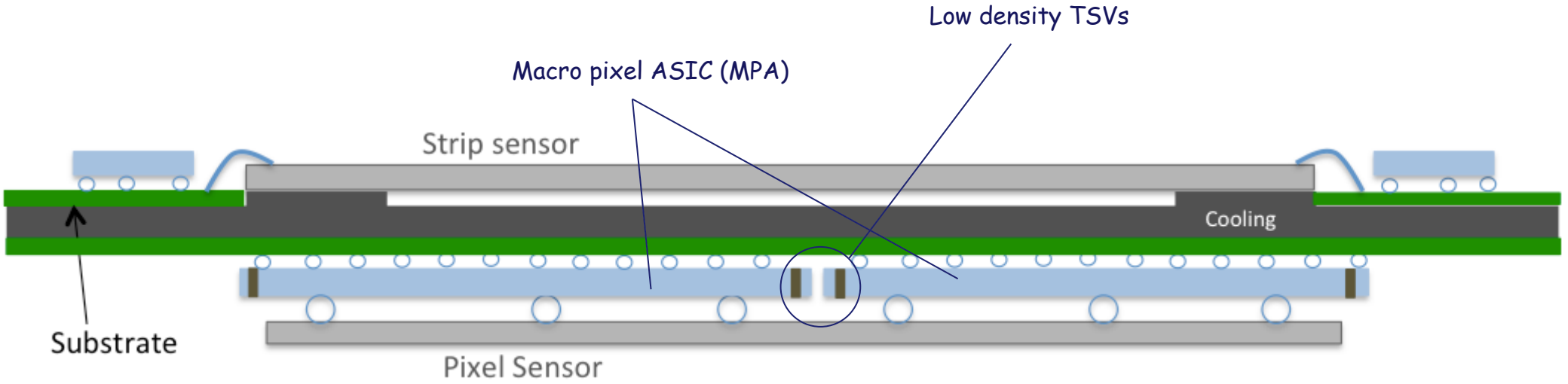


Prompt momentum discriminating tracker for HL-LHC



D. Abbaneo, A. Marchioro, "A hybrid cooling module architecture for a prompt momentum discriminating tracker at HL-LHC", JINST 7 C09001

- Provide information for Level-1 trigger processing, with local rejection of signals from low-momentum particles, by correlating signals in two closely spaced sensors
- Optimize p_t cut by tuning sensor spacing and acceptance window
- TSVs at the periphery of the pixel ASICs bridging two rows of chips in the middle to avoid regions of stub finding inefficiency



Conclusion

- Pixel detector requirements for next generation experiments at high luminosity colliders and X-ray sources are extremely challenging
  - high granularity ➔ small room for electronic circuits
  - high hit rate ➔ high speed, on-chip memory
  - data reduction ➔ hit discrimination capability
  - radiation hardness
- More functionalities need to be built into the readout chip to satisfy the specifications
  - front-end performance improvement
  - data selection and hit discrimination (bandwidth reduction)
- Technology evolution (both in the 'more Moore' and the 'more than Moore' sense) makes it possible to follow the trend and, actually, has a role in enhancing it, leaving room for creativity and continuous innovation

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