Oct 5, 2013

Advances in 3D silicon sensors

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Advances in 3D silicon sensors: lecture outline

- Section I
  - Introduction and basic principles
    - The 3D devices idea
    - Basic features
    - 3D device history
    - Basic technology
    - 3D devices performance
    - Applications: Examples and Exercises

- Section II
  - Advances for future 3D devices
    - Process and Layout optimization
    - Edge geometrical efficiency
    - Thin active region
    - Charge multiplication and 4D devices
    - Applications: Examples and Exercises

- Selected texts: Papers and Books

Advances in 3D-silicon sensors
Section I

Introduction and basic principles

The 3D devices idea

3D – A proposed new architecture for solid-state radiation detectors[1]

S.I. Parker[a],*, C.J. Kenney[a], J. Segal[b]

[a] University of Hawaii, Honolulu, USA
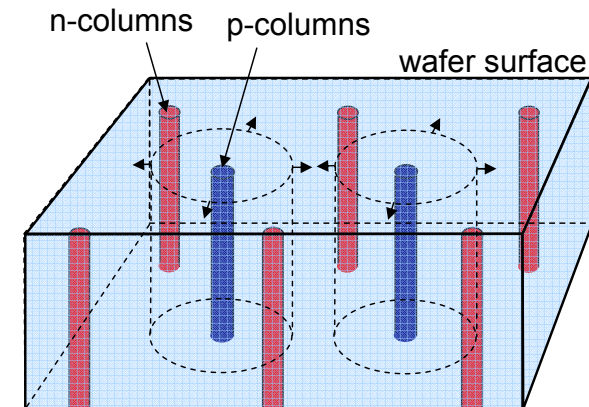[b] Integrated Circuits Laboratory, Stanford University, Stanford, USA

Pixel Cell layout
p⁻ bulk type

- Device with three-dimensional (**3D**) columnar electrodes which can have separations smaller than the sensor thickness, was developed **(1997)** to solve the problem of charge trapping in then-proposed *GaAs* sensors, a potential problem today for silicon pixel detectors in the inner layers at the LHC upgrade, the planned **HL-LHC** *(2020)*.

- List of main features:
  - Small collection distance
  - Very rapid charge collection
  - Quite low depletion voltages
  - Moderated Electrical field peak in critical places
 - Reduced charge sharing
  - ......
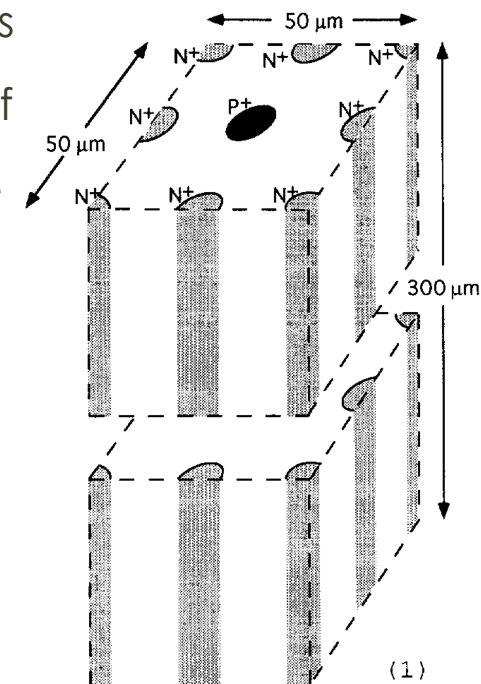
es: basic features... 1

n   p   n   p

electrodes

ndrical
pherical shape
n cylindrical
es of generally

ld for any given
ionization charges
ses.

n-columns   p-columns

wafer surface

- 3D vs Planar: Depletion volume grows along different directions
  - 3D: Orthogonal to silicon surfaces (E-field parallel)
 - Planar: Parallel to silicon surfaces (E-field orthogonal)

particle

n+   p+

electrodes

50 μm

depletion

particle

n+

300 μm

depletion

p+
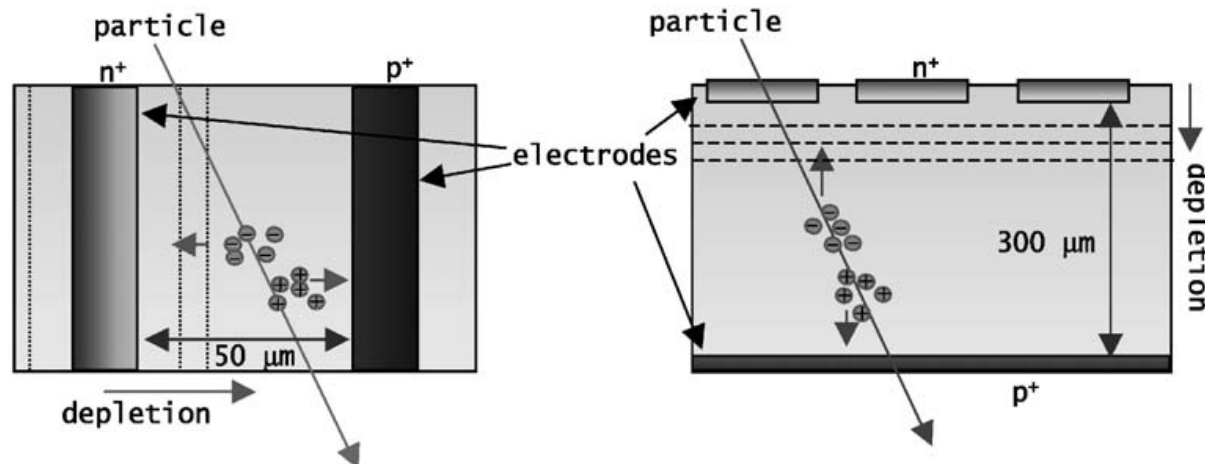
3D silicon devices: basic features... 2

- Collection distances (IES) can be as short as 50µm while the charge generated by the traversing particle can have much longer track lengths, depending on the application, by varying the substrate thickness.

  (as an example, 24000 e^-/h for a 300-µm-thick silicon substrate)

- Charge collection:
  - In a planar detector, each charge along the ionization path is at a different distance with respect to the collecting electrode, so the peak signal induction occurs at different times.
  - in a 3D detector the ionization path is parallel to the collecting electrodes. All charges along the path are at almost the same distance from the collecting electrodes. Ignoring some diffusion spreading, the arrival of all the charges is simultaneous, inducing a signal with a faster rise time with smaller spread.
    - Ten times faster response compared to a planar structure due to the shorter carrier drift distances.

3D   PLANAR

p^+ n^+ p^+ p^+

50 µm

300 µm

Inter Electrodes Spacing (IES)
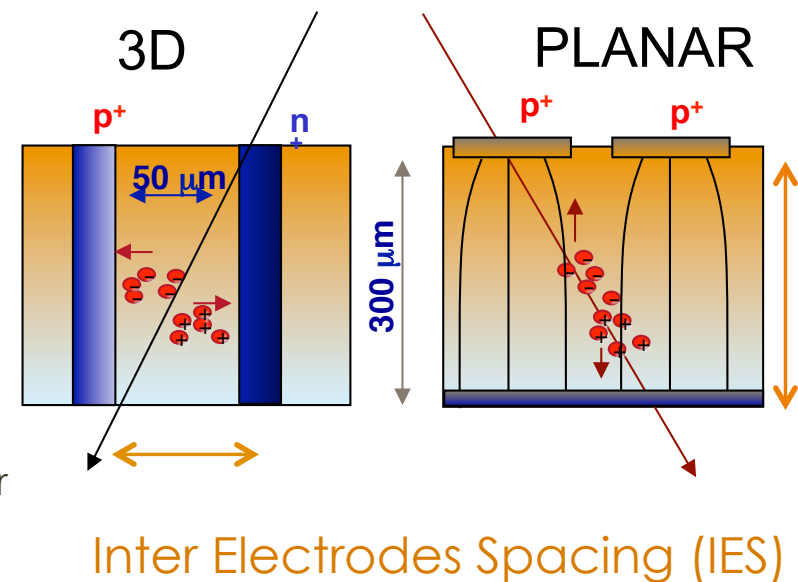
3D silicon devices: basic features... 3

- 3D devices have a non-uniform signal response due to the presence of low/null E-field regions between electrodes of the same doping type, and within the electrodes themselves.

  - Charge generated in these regions will initially move by diffusion (slowly), thus increasing the trapping probability (i.e. after radiation damage.)
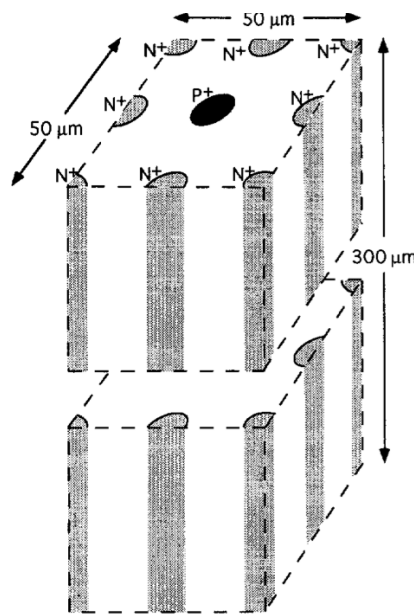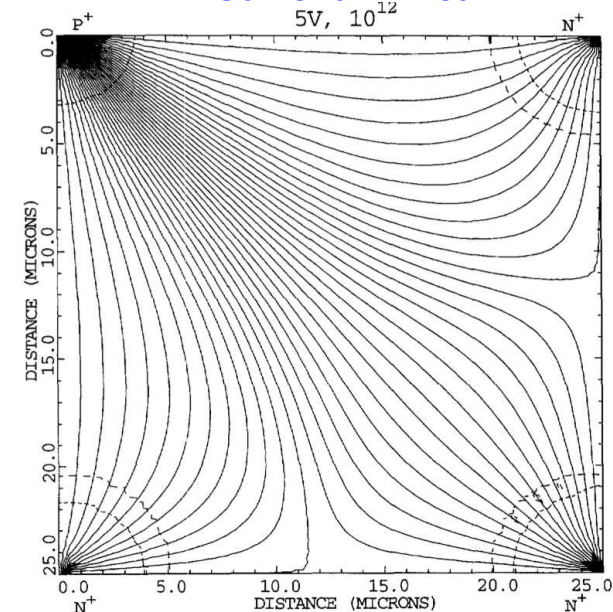
**Simulation
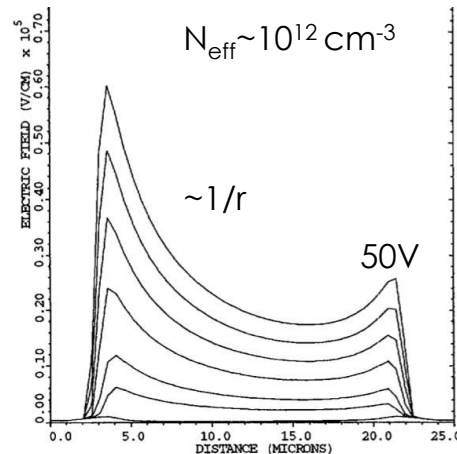Constant potential lines**
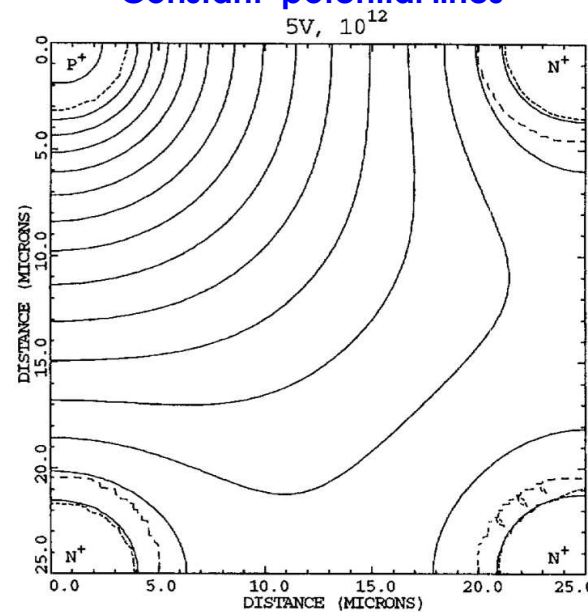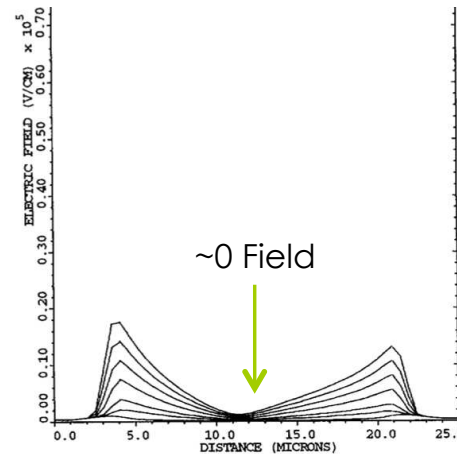
**Simulation
Carrier drift lines**

¼ of the cell

¼ of the cell

3D silicon devices: basic features... 4

Electric Filed (bias from 0 to 50V)

p+ to adjacent n+   n+ to adjacent n+
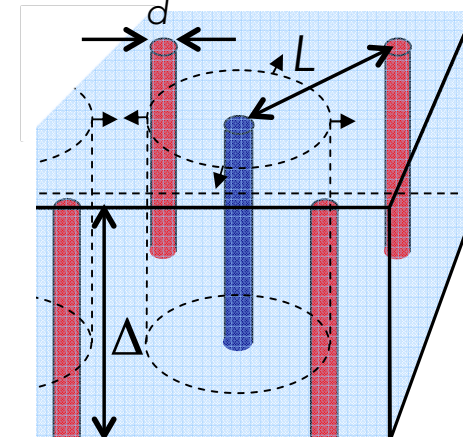
$N_{eff} \sim 10^{12}\, cm^{-3}$

~1/r

50V

~0 Field

- Electric field defined by
  - Electrodes shape and multiplicity
  - Bulk doping

- Depletion voltage can be calculated by (simplified) cylindrical approximation
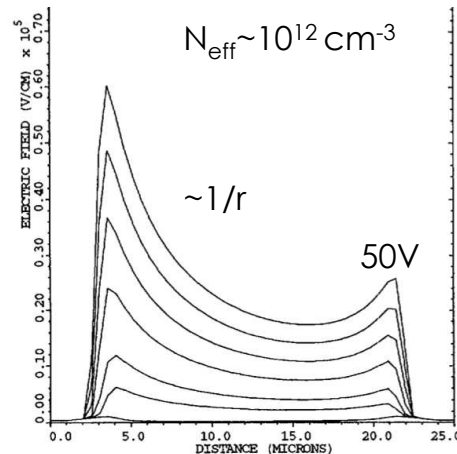
$$V_{depl} = \frac{qN_{eff}}{2\varepsilon_{Si}}\left[L^2\left(\ln\left(\frac{L}{d}\right) + \frac{1}{2}\right) - \frac{d^2}{2}\right]$$

d

L

Δ

3D silicon devices: basic features... 4

Electric Filed (bias from 0 to 50V)

p+ to adjacent n+   n+ to adjacent n+

$N_{eff} \sim 10^{12}\, cm^{-3}$

~1/r

50V

~0 Field

Planar Pixel   **3D Pixel**

$V_{FD}\ \alpha\ L^2$

- Electric field defined by
  - Electrodes shape and multiplicity
  - Bulk doping

- Depletion voltage can be calculated by (simplified) cylindrical approximation

$$V_{depl} = \frac{qN_{eff}}{2\varepsilon_{Si}}\left[L^2\left(\ln\left(\frac{L}{d}\right)+\frac{1}{2}\right)-\frac{d^2}{2}\right]$$
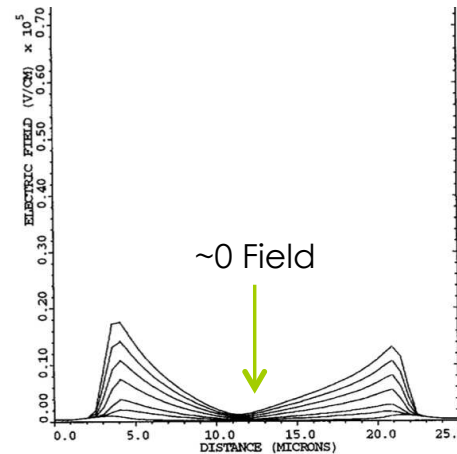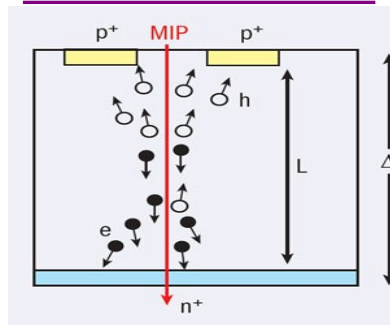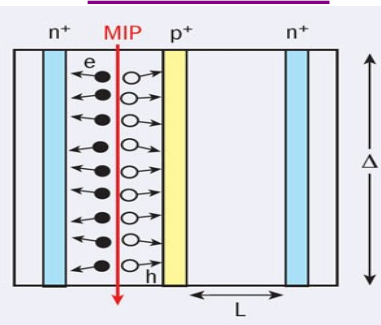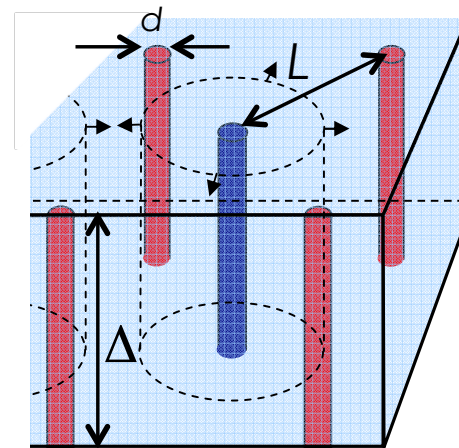
- Depletion voltage is defined by the Inter Electrodes Separation **"L"**
  - we expect smaller operational bias voltage for a 3D pixel compared to planar device

3D silicon devices: basic features... 5

- Electrodes geometry (i.e. diameter) is not only a technology driven choice: it affects the capacitance of a 3D device.
  - Electrodes capacitance should be larger than the one of a standard planar device, because of the **shorter inter-electrode separation** and **the extension** of the electrodes all the way through the silicon bulk.
    - Affects the signal and the noise of a 3D detector
  - Simplified calculation can predict the main features of geometrical capacitance:
    - Capacitance proportional to Δ (electrodes length)
    - inversely (ln) to the IES =L
      - Larger IES worsen charge collection performance
    - Should improve for smaller d
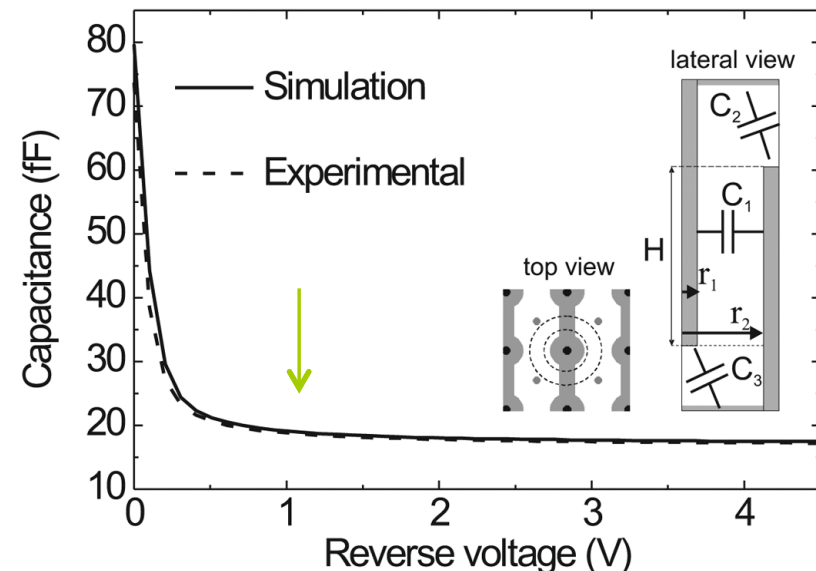   - This increases the E-Field at junctions

$$C = \frac{\pi \varepsilon_{si}}{\ln \dfrac{2L}{d}} \Delta$$ If L >> d
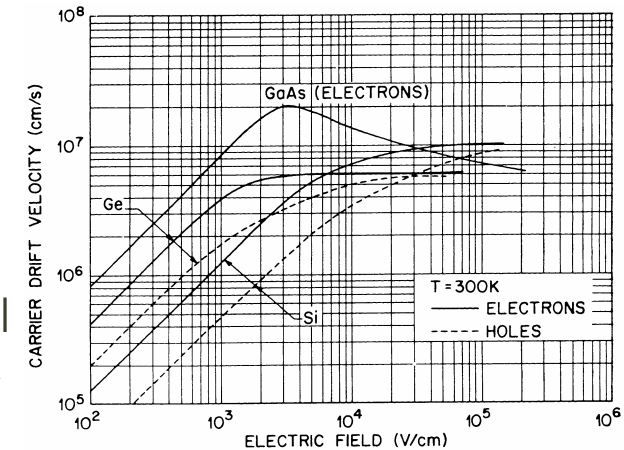
3D silicon devices: basic features... 5

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    - Should improve for smaller d
      - This increases the E-Field at junctions

$$C = \frac{\pi \varepsilon_{si}}{\ln \dfrac{2L}{d}} \Delta$$

If L >> d

$$V_b > V_d$$

$$E(x) = -\frac{q\,N}{11\,\varepsilon}(w - x) \equiv E\,(w - x)$$

$$v(x) = \mu E(x) = \mu E\,(w - x)$$

3D silicon devices: basic features... 6

- Carrier velocity saturate at high field (at E~3 10^2 KV/cm mobility ~ 1/E)
  - *e⁻* saturation speed of ~100 µm/ns
  - *h* saturation speed of ~80 µm/ns

- We expect a short collection time, so the signal formation to the electrodes will have fast peak
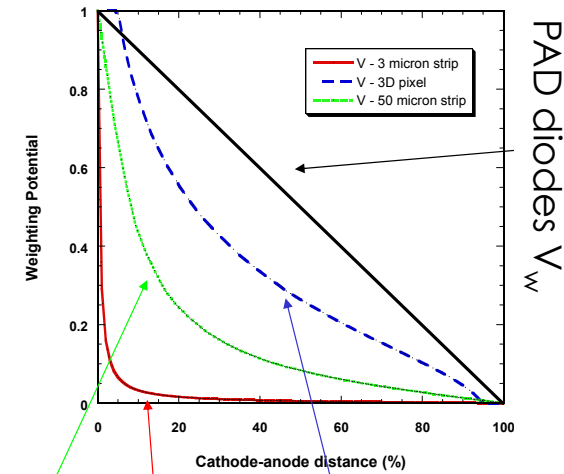 - ~1/4 ns for the fastest component

Carrier drift simulation: a m.i.p. parallel to electrodes
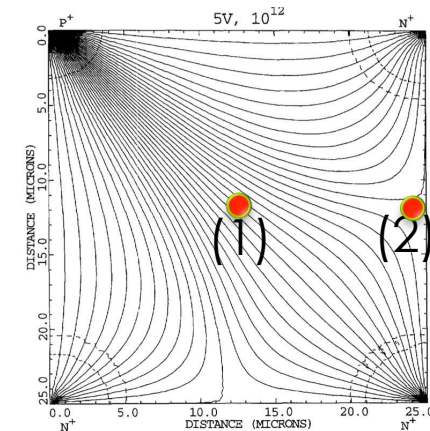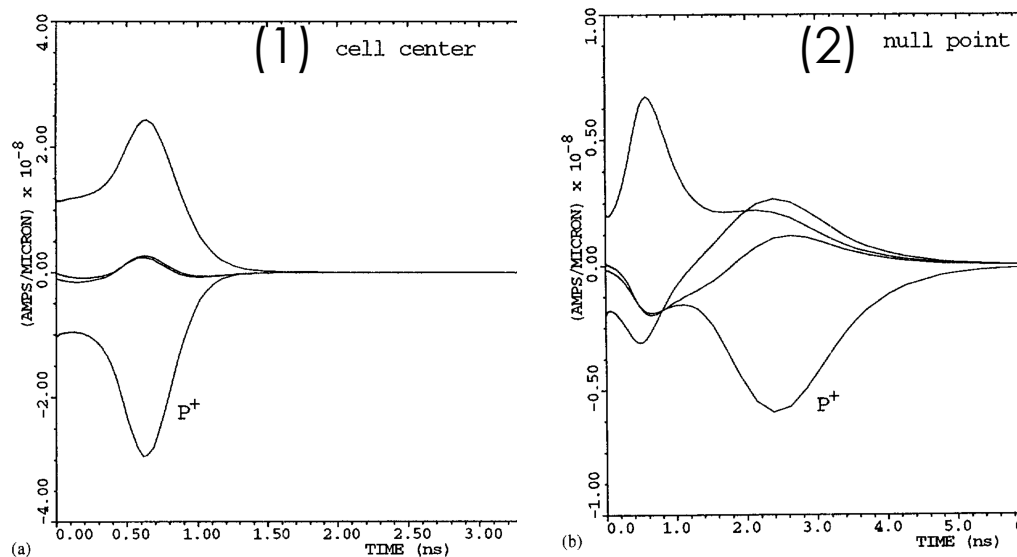
3D silicon devices: basic features... 6

- "Ramo" theorem: Signal to the electrodes is proportional to the speed
  - $i(t)$ = -q v(t) E_w
  - E_w and V_w depends on electrodes geometry
    - 3D like PAD diodes

- Charge collected (*e* or *h*) to the electrodes is proportional to the speed, and can be reduced by carrier trapping (τ_{eff})
  - $\lambda = \tau_{eff} v_d$ (different for *e* or *h*)

- Easy calculation for "pad" like detector: unitary primary carrier charge created at distance x from collecting electrode
  - $dV_w/dx = 1/L$ L=IES

- The Signal Efficiency SE=S/$N_{carrier}$
  A m.i.p. signal uniformly distributed through the bulk

- **e or h 3D Signal Efficiency (L $\leq \lambda$) $\geq$ 37 %**
  - SE~λ/L   if λ/L $\leq$ 1 (i.e. for planar after radiation damage)

$$i(t) = \frac{dS}{dt} = q\frac{dV_w}{dx}\frac{dx}{dt}e^{-\frac{x}{\lambda}}$$

$$S = \frac{\lambda}{L}\left[1 - e^{\frac{x}{\lambda}}\right]$$

$$SE = \frac{\lambda}{L} - \left(\frac{\lambda}{L}\right)^2 + \left(\frac{\lambda}{L}\right)^2 e^{-\frac{L}{\lambda}}$$

3D Devices: history

- 1985: Proposal to drill column on a silicon wafer
- 1997: First proposal of a 3D device
- 1999: First fabrication of 3D device
- 2001: First results with special edges (active) in 3D device
- 2003: First results of irradiated 3D device

……

- 2010: 3D detector become a technology for the ATLAS-IBL Upgrade

……

- 2015 first collision tracks will be reordered by 3D detector

After more than 10 years from the first device proposal the 3D devices are today a viable solution for a pixel particle detector

4 inch wafer   **4 inch wafer**

(a)   (b)

How to build a 3D device: Basic technology

- Since the proposal ~ 5 generation of 3D devices have been produced. Many improvements/simplification are done and more silicon manufacturers are today on the game.
- Variety of processing methods developed
  - The original full-3D design fabricated at Stanford [1] and in parallel at SINTEF in Oslo [2], with fully penetrating electrodes, has been complemented by a modified-3D design by FBK-Irst in Trento[3] and CNM in Barcelona [4] in which the electrodes do not penetrate the entire substrate thickness.

[1,2]   [3]   [4]
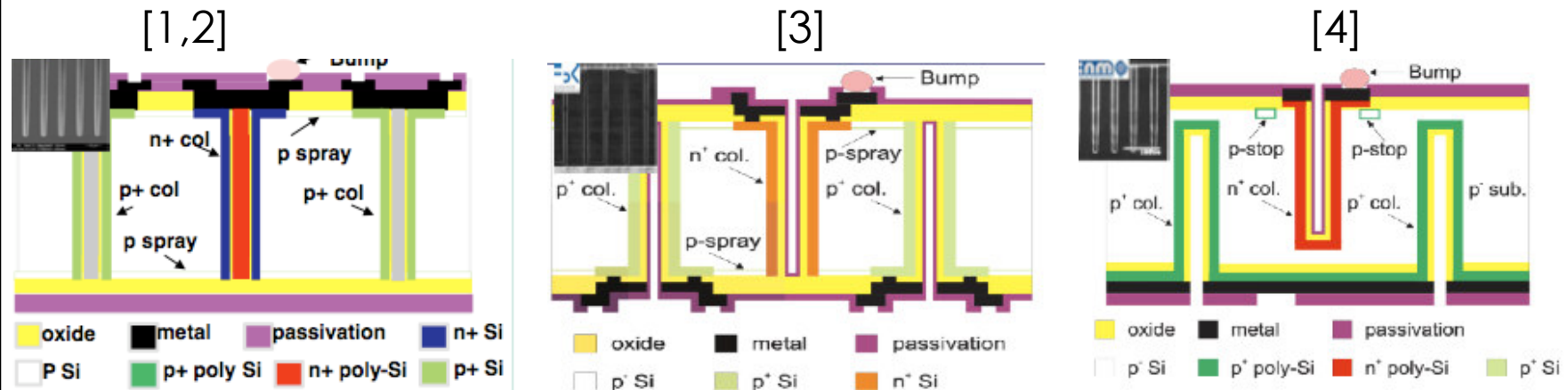
[1] C. Kenney, S. Parker, J. Segal, and C. Storment. IEEE Trans. Nucl. Sci. , VOL. 46, NO. 4, AUGUST 1999
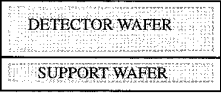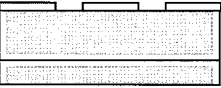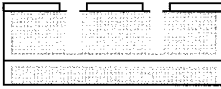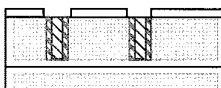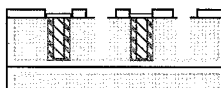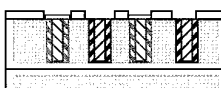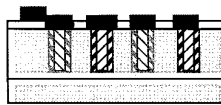[2] T.E. Hansen, et al., J. Instr. 4 (2009) P03010
[3] A. Zoboli, G.F. Dalla Betta, M. Boscardin, C. Piemonte, S. Ronchin, N. Zorzi,L. Bosisio, IEEE Trans. Nucl. Sci. NS-55 (2008) 2775
[4] G. Pellegrini, M. Lozano, M. Ullan, R. Bates, C. Fleta, D. Pennicard, Nucl. Instr. and Meth. A 592 (2008) 38.

How to build a 3D device: Basic technology

- The fabrication of a 3D device implies process for etching narrow holes with high precision through the silicon bulk.
  - First attempt was to build 3D diodes by laser drilling and diffusion [1].
  - Today the technology combines micro-machining and standard Very Large Scale Integration (VLSI) processing
  - Optimized solution is by using deep reactive ion etching (DRIE) [2]
  - Exploit the high-precision etching techniques in silicon

TABLE II

FABRICATION STEPS—SCHEMATIC CROSS SECTION DIAGRAMS. THE DIAGRAMS ARE SHOWN AFTER EACH SET OF STEPS. NEITHER THE WAFERS NOR THE STRUCTURES ARE TO SCALE. THE SUPPORT WAFER WAS THICKER THAN THE DETECTOR WAFER, BUT WITH NO STRUCTURES TO SHOW IT WAS MADE SMALL TO SAVE SPACE

| DETECTOR WAFER | STEPS 1 - 3 |
| SUPPORT WAFER | OXIDIZE AND FUSION BOND WAFERS |

STEPS 4 - 6
PATTERN AND ETCH P⁺ WINDOW CONTACTS

STEPS 7 - 8
ETCH P⁺ ELECTRODES

STEPS 9 - 13
DOPE AND FILL P⁺ ELECTRODES

STEPS 14 - 17
ETCH N⁺ WINDOW CONTACTS AND ELECTRODES

STEPS 18 - 23
DOPE AND FILL N⁺ ELECTRODES

STEPS 24 - 25
DEPOSIT AND PATTERN ALUMINUM

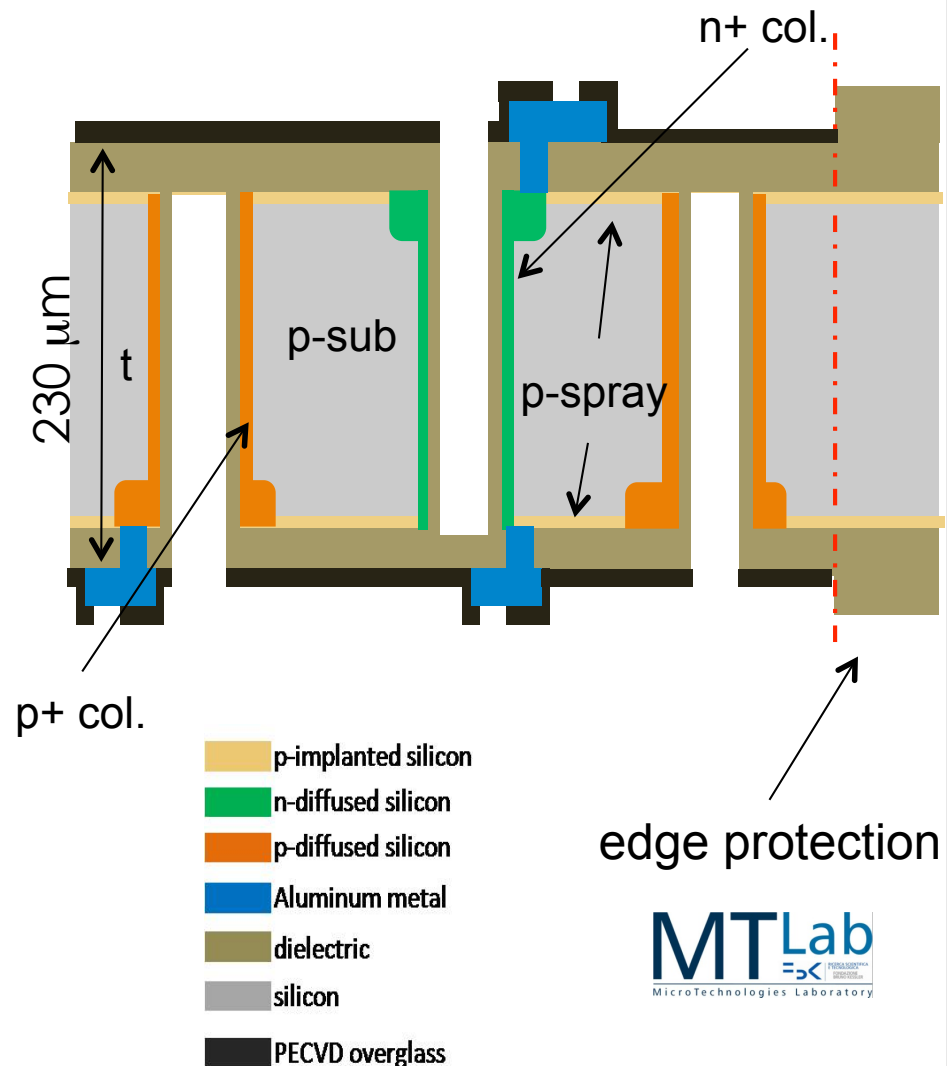*Rather challenging process for a mass production*

[1] J. Appl. Phys. **53**, 9154 (1982); doi : 10.1063/1.330427
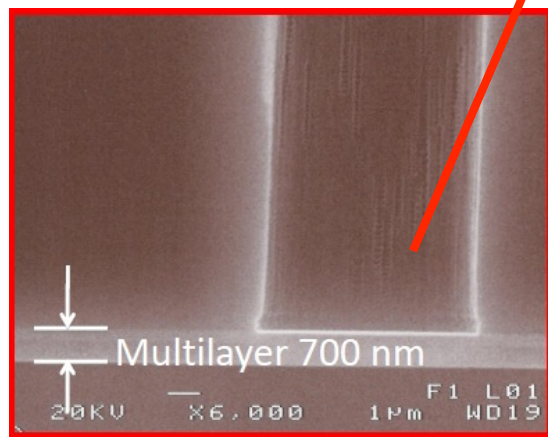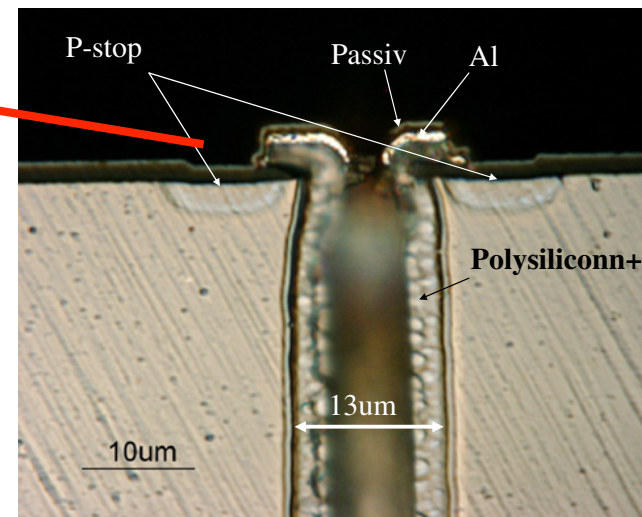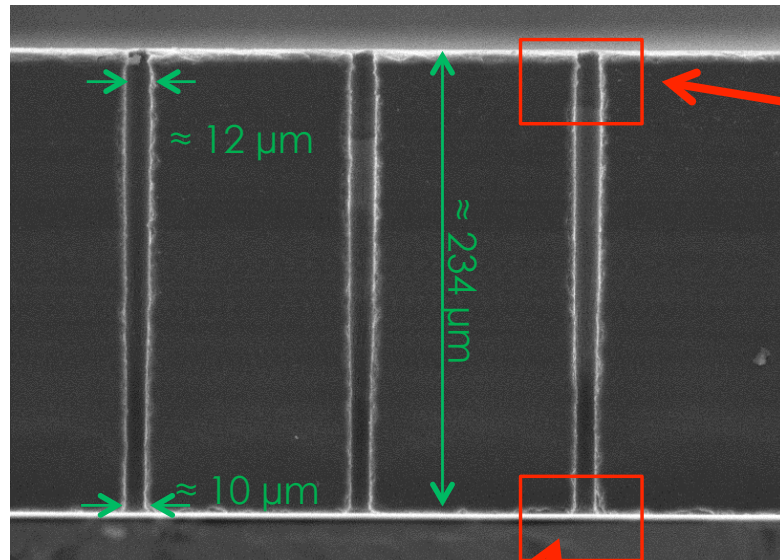Deep Reactive Ion Etching
[2] Sensors and Actuators A 144 (2008) 109–116 doi:10.1016/j.sna.2007.12.026

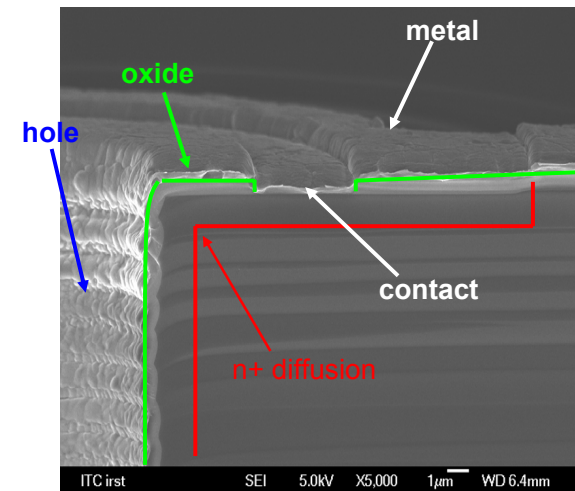# 3D-DTC with passing through columns: simplify process

- Column depth equal to the wafer thickness, etched from both sides
  - Deep RIE
- Full double side process
  - No support wafer
- Surface isolation with p-spray on both sides
- Columns (~12 µm diam.)
  - "empty", doped by thermal diffusion and passivated by SiO_2
  - Poly silicon filled (LPVDC with SiH_4)

- Edge protection in order to improve the mechanical yield

- Wafer deformation: critical bow for processing and IV performance

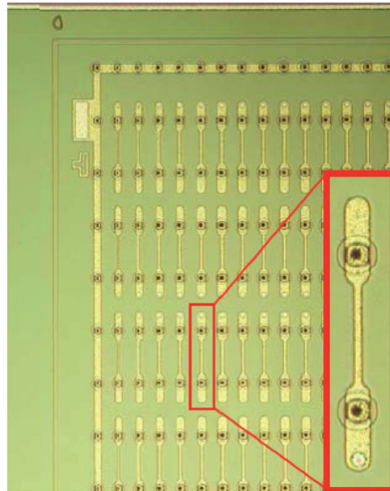- Aspect ratio: depth to width ratio
  - 20

230 µm

t

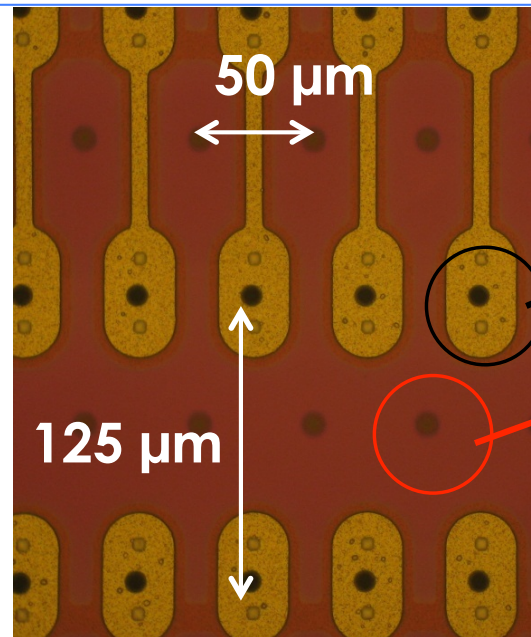p-sub

n+ col.

p-spray

p+ col.

edge protection

Legend:
- p-implanted silicon
- n-diffused silicon
- p-diffused silicon
- Aluminum metal
- dielectric
- silicon
- PECVD overglass

MT Lab
MicroTechnologies Laboratory

3D columns: pictures

P-stop   Passiv   Al

Polysiliconn+

10um

Multilayer 700 nm

20KV   X6,000   1µm   WD19

Etch stop for DRIE

metal

oxide

hole

contact

n+ diffusion

ITC irst   SEI   5.0kV   X5,000   1µm   WD 6.4mm

3D device: Layout details for hybrid pixel assembly

50 µm

125 µm

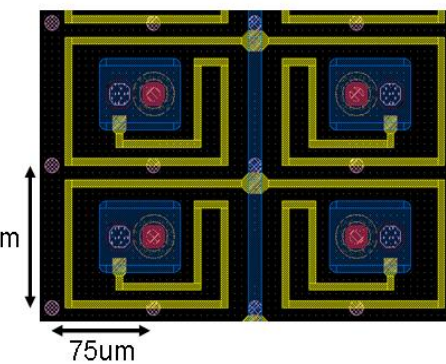*Junction side*
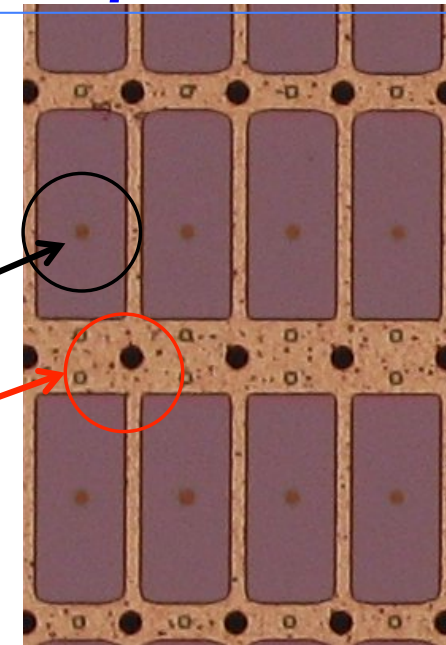
Ohmic Side
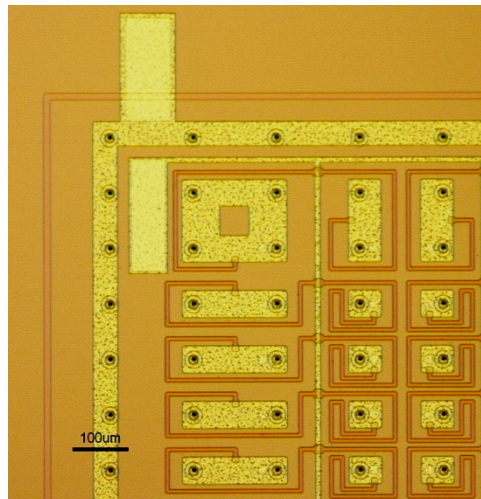
Dense → Expected higher radiation resistance
Sparse → Expected lower noise

100um

150um

75um

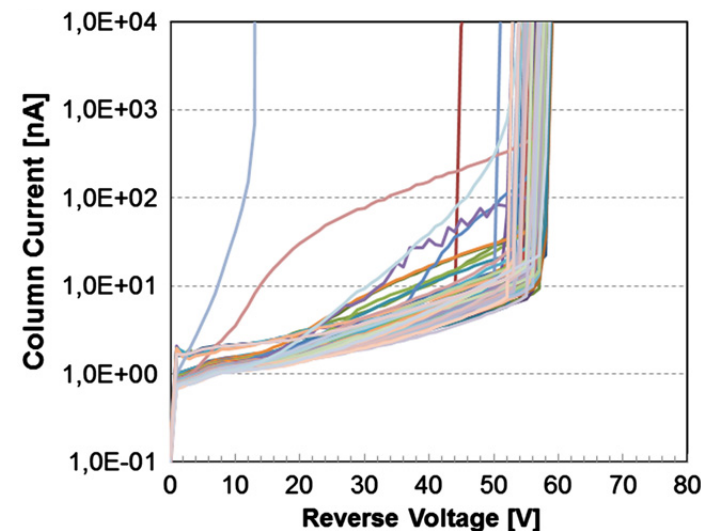10um

100um

MT**Lab**
MicroTechnologies Laboratory
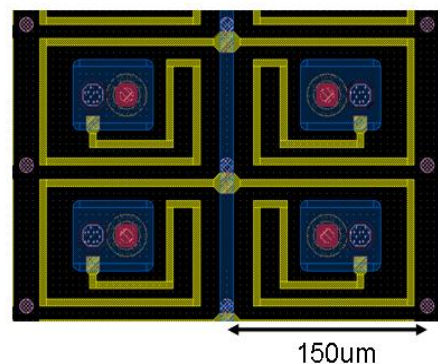
3D detector performance: before irradiation …1

- Operation of 3D devices as detectors implies
  - Bias voltage beyond full depletion
  - Stability : I leakage vs time
    - A single column defect can discard a full detector for early breakdown

Sintef: ATLAS IBL
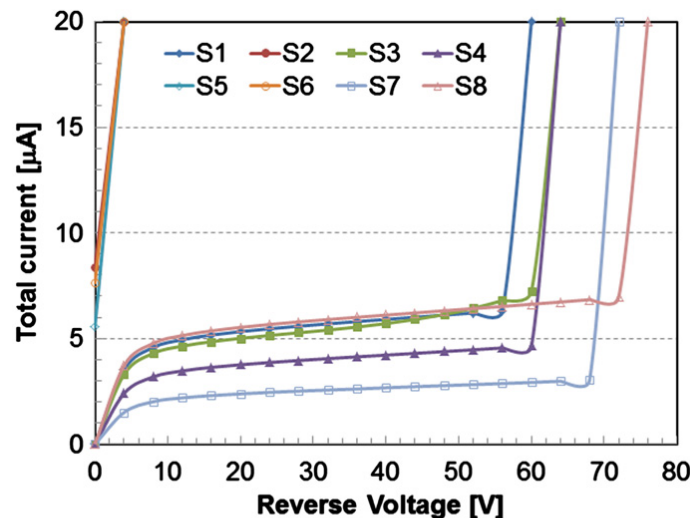
FBK: ATLAS IBL

- Process step optimization for a stable and robust technology
  - Crucial production yield
    - Today we have large variation : min 44 % ….. max 88 %

# *3D detector performance: before irradiation …2*

- 3D sensors by design exploit a self-shielding effect within a cell
  - Best for a binary readout
- charge sharing between adjacent cells is considerably reduced as compared to planar sensors
- In 3D sensors, however, the magnetic and electric fields are co-planar which minimizes considerably the effect of the magnetic field.

PLA=planar pixel
STA=poly filled column 3D
*Beam test data* FBK=empty column 3D
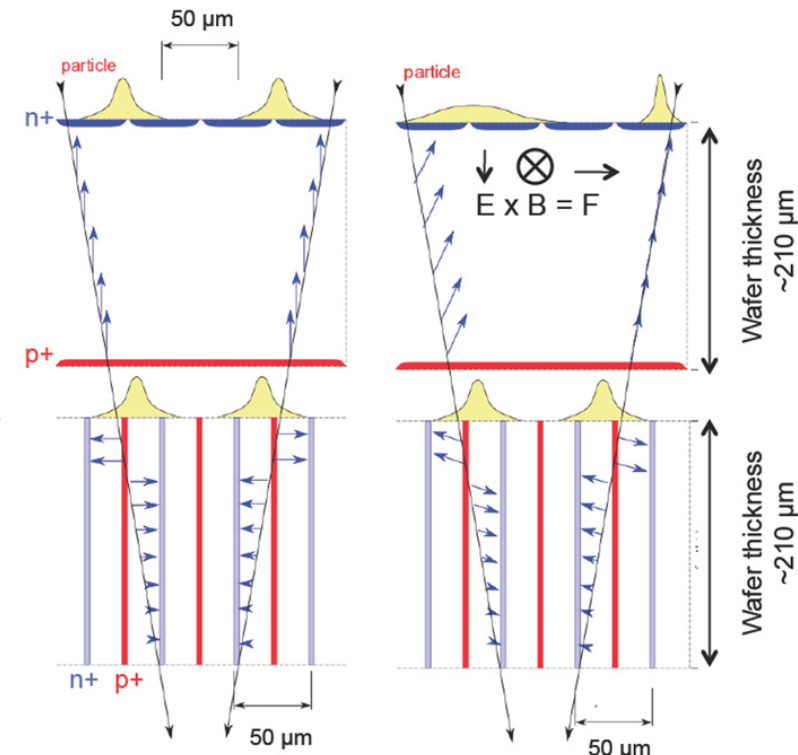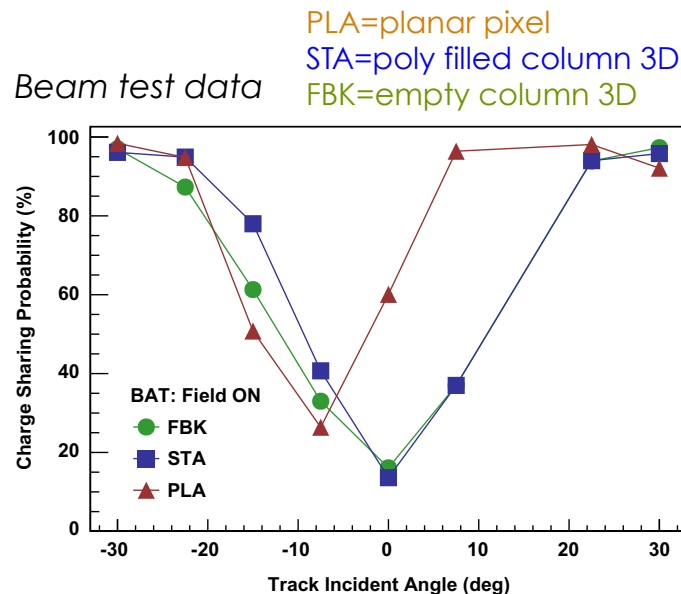
- Lorentz angle carrier drift in magnetic field is less effective for 3D sensors
  - The sharing probability is symmetrical around the orthogonal incidence
    - Increases crossing the 3D cell
  - For planar sharing is minimized for track paths along the Lorentz angle direction

3D detector performance: before irradiation …3

- Tracking efficiency and resolution are fundamental features of pixel detectors.
  - Tracking efficiency is defined as the probability of finding a hit close to a track.
    - 3D sensors are not 100 % efficient for normal incident tracks: the column volume and the "zero" field regions affect the efficiency
      - Given the high aspect ratio of the electrodes, track length inside electrodes is small for inclined tracks, enough charge can be collected in the bulk region to recover efficiency.

- In application to experiment with solenoidal magnetic field the detection efficiency can be recovered, by track curvature:
  - 3D empty column electrodes (FBK) show high efficiency, greater than poly filled ones (STA): the electrodes penetrate/diffuse fully the sensor bulk volume decreasing the collection volume size.
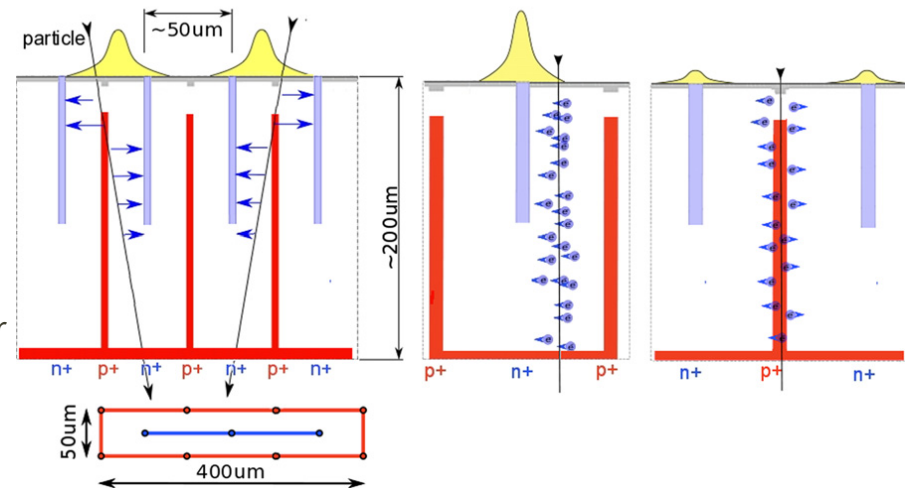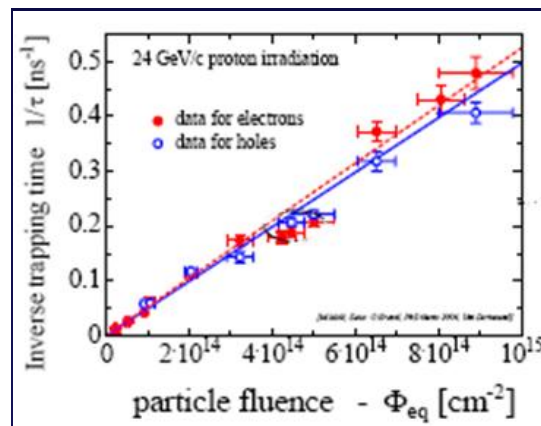
Beam test data
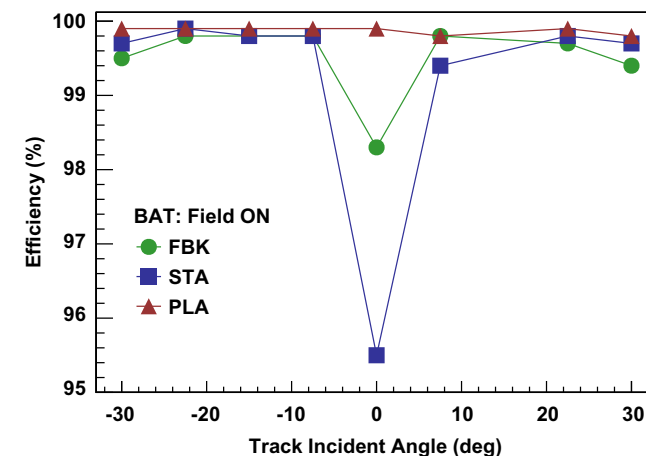
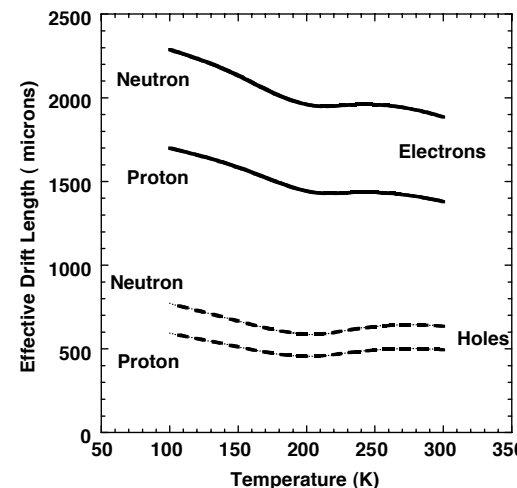# *3D device performance: after irradiation …1*

- Charge collection after high level of radiation damage is one of the main issues
  - Primary charges are trapped along their drift path by bulk defects
    - The effective trapping time t_{eff} decreases as the radiation defect density increases
    - $\lambda_{eff} = V_{drift} \times t_{eff}$ define the trapping length

Trapping time decreases ~linearly with fluence

$$\frac{1}{t_{eff}} = \frac{1}{t_o} + K_\tau \Phi$$

λ_{eff} at fluence 10^{14} n_{eq}/cm^2 at bias 10^4 V/cm

λ_{eff} Scaling to HL-LHC fluences (10^{14} n_{eq}/cm^2) T=-20°C

Fluence	1	10	100
Carrier	λ (Proton)	λ (Proton)	λ (Proton)
e	~1500 μm	~150 μm	~30 μm
h	~500 μm	~50 μm	~10 μm

$$\frac{dS}{dt} = q\frac{dV_w}{dx}\frac{dx}{dt}\exp(-\frac{x}{\lambda})$$

- 3D detectors should perform better compared to planar devices
  - charge collection distance (λ) and substrate thickness (Δ) are decoupled
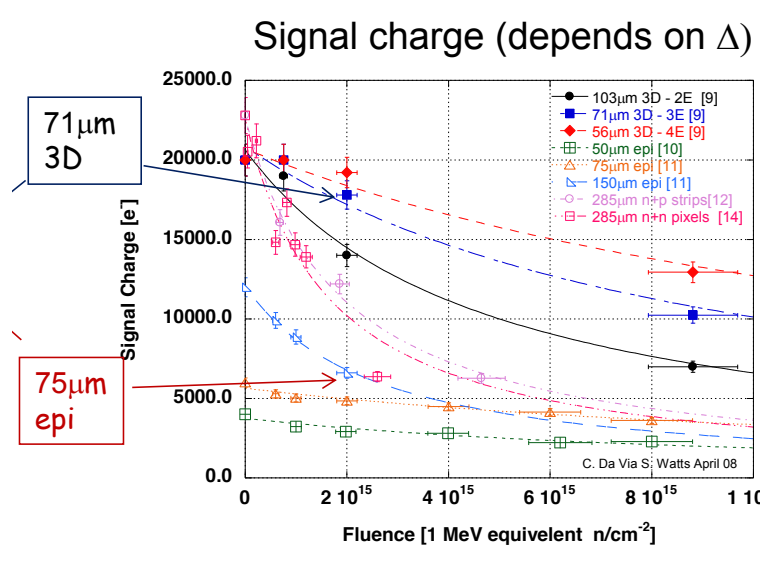   - λ can be optimized according to the radiation hardness ($\Delta \sim \lambda_{eff}$)

$$S = \frac{\lambda}{\Delta}\left[1 - \exp(-\frac{x}{\lambda})\right]$$

3D device performance: after irradiation ...2

- Performance compared to planar with similar IES

C. Da Via S. Watts April 08

[9] C. Da Via et al.", (NIMA-D-08-00587)
[10] G. Kramberger at al., Nucl. Instr. Meths. A 554 (2005) 212-219
[11] G. Kramberger, Workshop on Defect Analysis in Silicon Det, Hamburg, August 2006. http://wwwiexp.desy.de/seminare/defect.analysis.workshop.august.2006.html
[12] G. Casse et al., Nucl. Instr. Meths. A (2004) 362-365
[14] T. Rohe et al. Nucl. Instr. Meths. A 552 (2005) 232-238
[16] F. Lemeilleur et al., Nucl. Instr. Meths. A 360 (1995) 438-444

Inter Electrodes Spacing (IES)

$$SE = \frac{1}{1 + 0.6\lambda \frac{K}{V_{drift}} \Phi}$$

C. Da Via S. Watts April 08
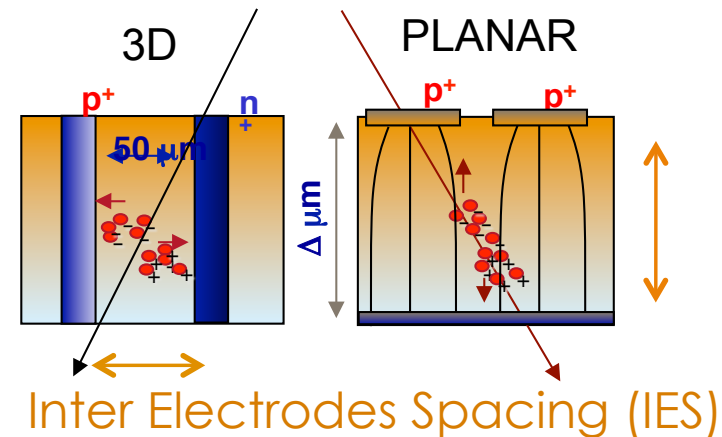
Simple example at 10^{16} ncm^2

Δ=substrate thickness
λ= <trapping distance>~30um

S_{MIP} planar ~ 80 (Δ/IES) x Δ ~ 80λ ~ 80x30 ~ 2400e$^-$

S_{MIP} 3D ~ 80λ x (Δ/IES) ~ 2400 x 210/(71-22$_{electrode\ implant}$) ~ 10290e$^-$

# *3D device performance: after irradiation ...3*

- Signal speed after irradiation (..... and also noise , capacitance , stability)
  - An IR laser (1064 nm, pulse width of 0.1 ns) was used to scan the devices with the spot focused on the centre of the bulk silicon. The spot had a diameter with a FWHM equal to 7μm.
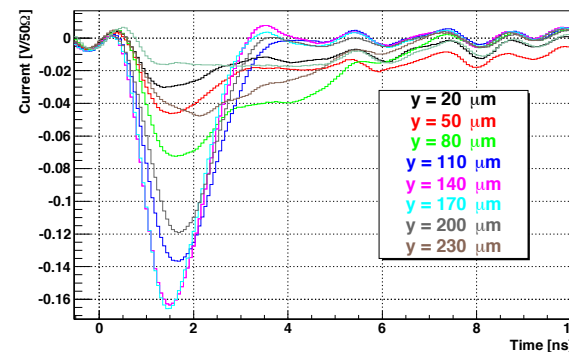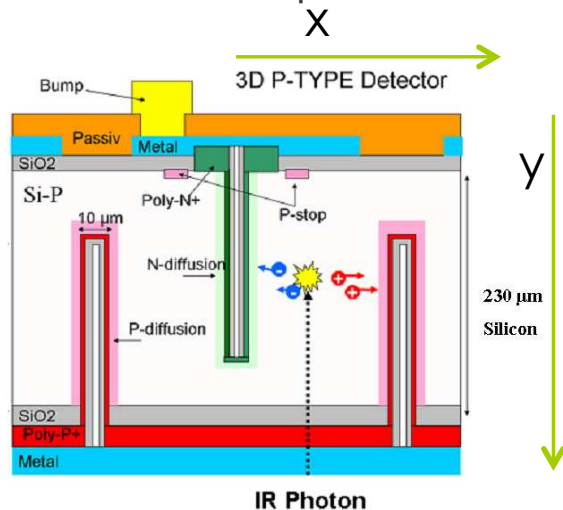
- Before irradiation
  - Signal collection faster in the inter-column position (y-center)

- After heavy irradiation (5 10^{15} n_{eq}/cm^2)
  - Signal collection speed decreases
  - Recovered after defect annealing
    - Improved speed given the higher operational bias
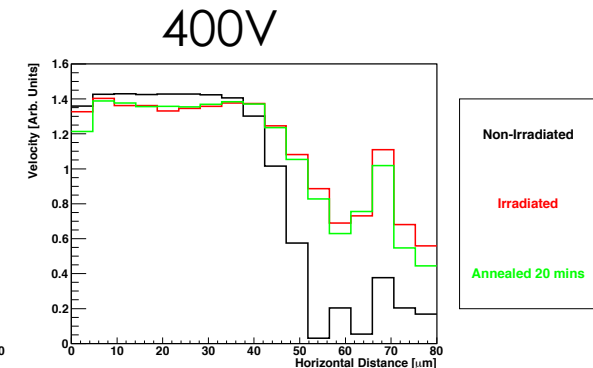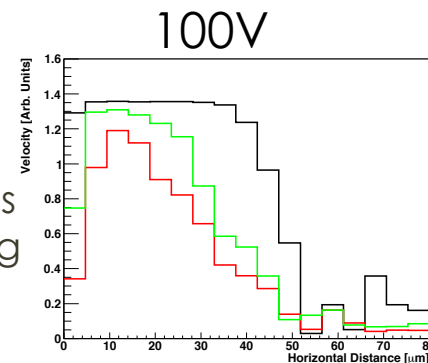
Examples and exercises

○ Calculate maximum time-spread of a m.i.p. within a 3D cell

○ Colum electrodes:
  ○ Electrodes can be "empty", poly-silicon or Epitaxial silicon filled
    ○ Discuss pros and cons
  ○ How much C affect collected signal?
  ○ Measure column capacitance C after radiation damage

○ Derive the approximate expression for
  ○ Depletion voltage

○ Signal Efficiency
  ○ 3D pixel efficiency vs collection distance
    ○ Calculate maximal IES admissible
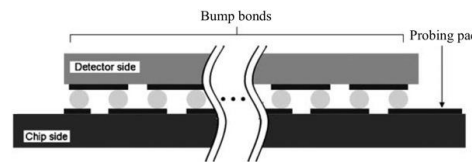   ○ Derive SE formula after radiation damage

Advances in 3D-silicon sensors
Section II

Advances for future radiation tolerant devices

3D advances for future pixels

- Advances in Read Out Chip (ROC in 65 nm technology) for hybrid pixel detectors allow the design of smaller pixel:
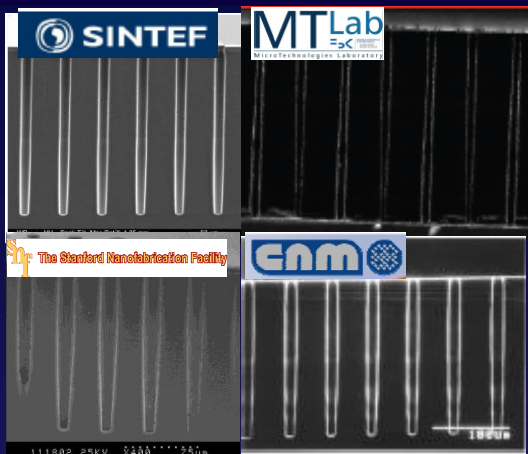 - Today : 400 X 150 μm^2 ; Future: 150 x 25 μm^2

  - thinner sensor or smaller collecting charge thickness to take advantage of the improved pixel spatial resolution: smaller cluster size per track also for large incidence angle
  - Thinner device for a reduced material budget

- Smaller Inter Electrode Spacing for radiation hardness qualified for extreme radiation hardness
  - High operational voltage
  - Today radiation tolerance of 3D detectors
    - $\Phi \sim 5 \; 10^{15} \; n_{eq}/cm^2$: 70 μm IES
  - Future radiation tolerant 3D detectors
    - $\Phi \sim 2 \; 10^{16} \; n_{eq}/cm^2$: optimized IES $\leq$ 50 μm
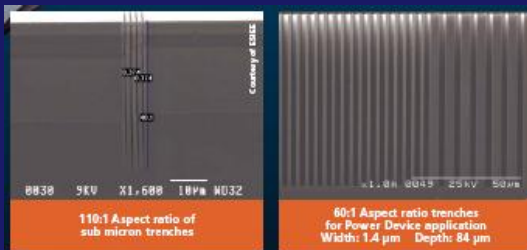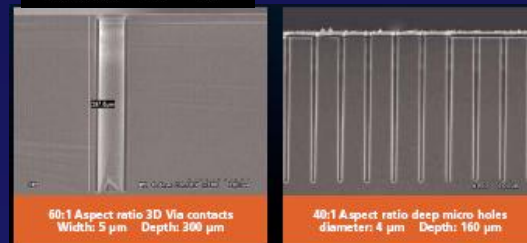
3D advances for future pixels

- Implications:
  - Higher column density and bump density
    - Narrower electrodes are needed
      - decrease geometrical inefficiency of electrodes and lower capacitance (noise)
        - Thinner substrate allow to maintain constant Aspect ratio and to decrease the capacitance
        - Thin electrodes in thin substrate can be easily filled with Poly silicon , increasing the column efficiency
          - More readout electrodes connected to the same ROC channel.

  - Sensor thickness to be optimized (depending on signal/threshold)
    - case 1 ~ 150 μm: feasible with "passive" sensor
    - case 2 < 100 μm: charge multiplication necessary

  - Very slim (or active) edges for hermetic coverage

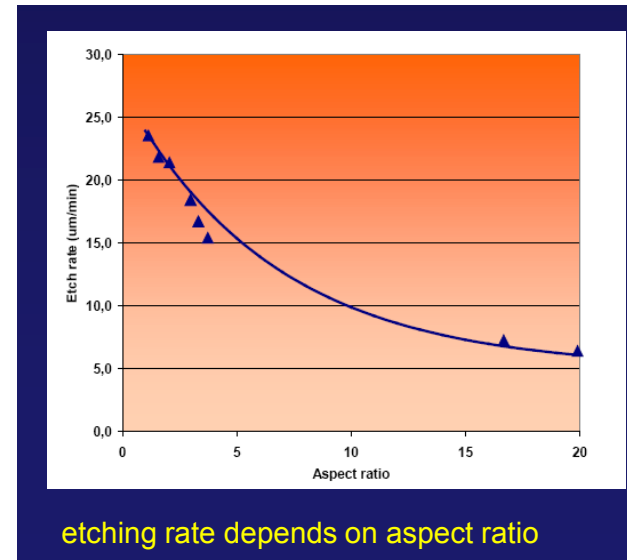# 3D Process and Layout: DRIE and Aspect (depth/width) ratio

1997 10:1

2010 24:1

60:1

110:1

60:1 Aspect ratio 3D Via contacts
Width: 5 μm   Depth: 300 μm

40:1 Aspect ratio deep micro holes
diameter: 4 μm   Depth: 160 μm

110:1 Aspect ratio of
sub micron trenches

60:1 Aspect ratio trenches
for Power Device application
Width: 1.4 μm   Depth: 84 μm

"SHARP"
SUPER HIGH ASPECT RATIO > 110:1

ALCATEL
Micro Machining Systems

UNIQUE ALCATEL DRIE PATENTED PROCESS

etching rate depends on aspect ratio

- Trend for new tracking detectors:
  - Small pixels (50 X 125 μm^2)
    - High bump density
  - Thinner bulk: constant Aspect ratio
    - Under control load C
  - Smaller V_{fd}
  - Faster signals
  - Smaller collection distances

3D Process and Layout: design optimization

- Relatively low intrinsic breakdown voltage
(p-spray related, well understood)
- Might be an issue for post irradiation performance
- High sensitivity to process defect (a single defect kills an entire sensor)
- High yield variability
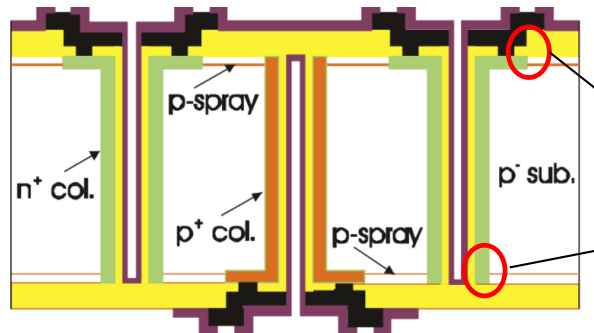
- Simplified process seems promising: significant improvement on breakdown voltage
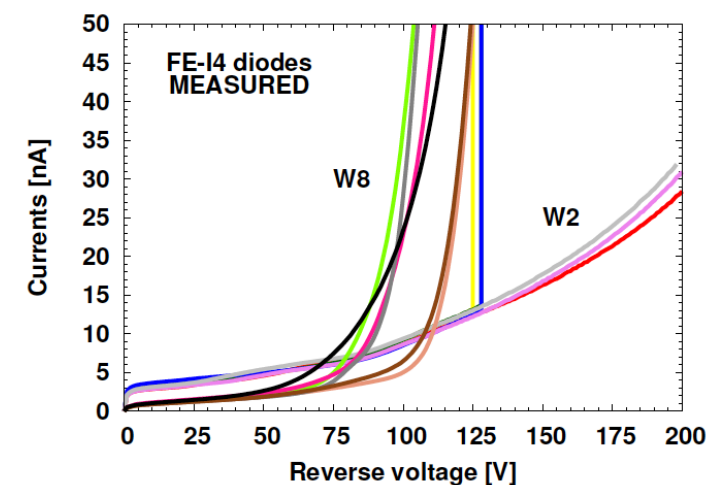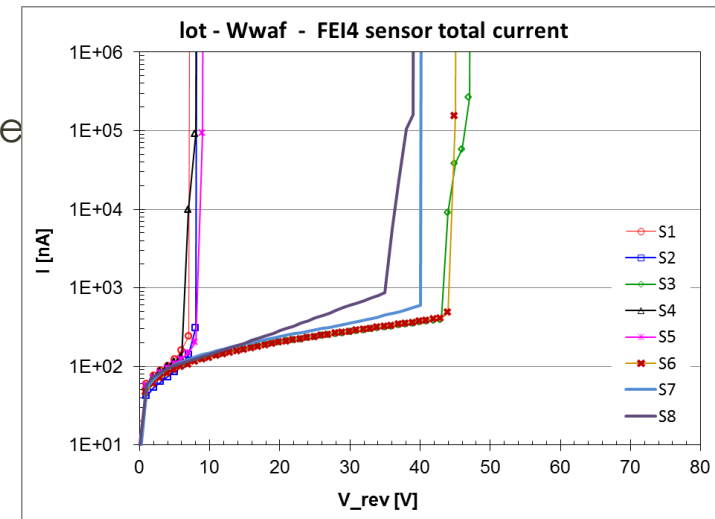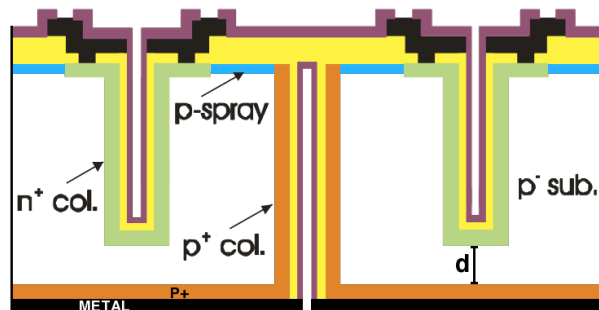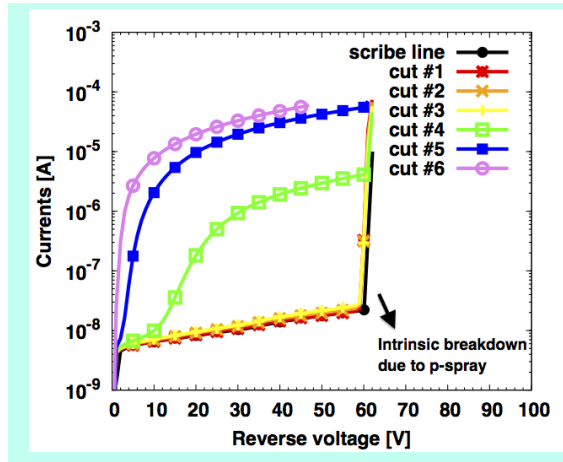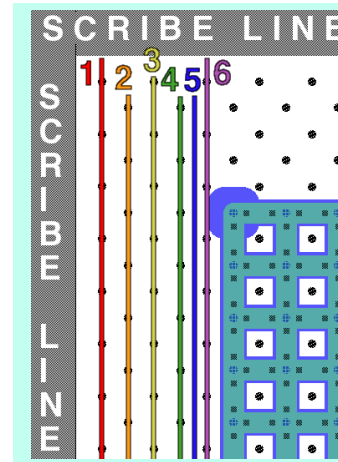
3D Edge geometrical efficiency

- Slim and Active edges were made by etching a trench around the detector's physical edge and then diffusing in dopant to make an electrode. The electric field lines, which are parallel to the wafer's surface, can then be properly terminated at this ''edge'' electrode.

- Normally these processes require the use of a support wafer that provides mechanical strength and supports the devices during and after the active edge etch. The removal of this support takes place after a dicing etch, which penetrates the device wafer and completely surrounds each device perimeter.

Passivation   Aluminium
Isolation oxide
n-type epi-Si   Trenches filled
                                 with poly-silicon
Si bulk p^+
n^+

Substrate thinning
(a thin layer of heavily doped substrate is left)

thin n^+ layer

Device separation along the trenches

- Some advantages of slim/active edges are:
    - The edge leakage current, usually present after the device has been saw-cut, is suppressed.
    - The dead area which would be otherwise needed for guard rings, chips and cracks resulting from sawing, and to control the bulge of the electric field in planar detectors is reduced to no more than a few microns.
- 3D devices have a sort of "by design" protection provided by the column and electric field intrinsically parallel to the wafer surface
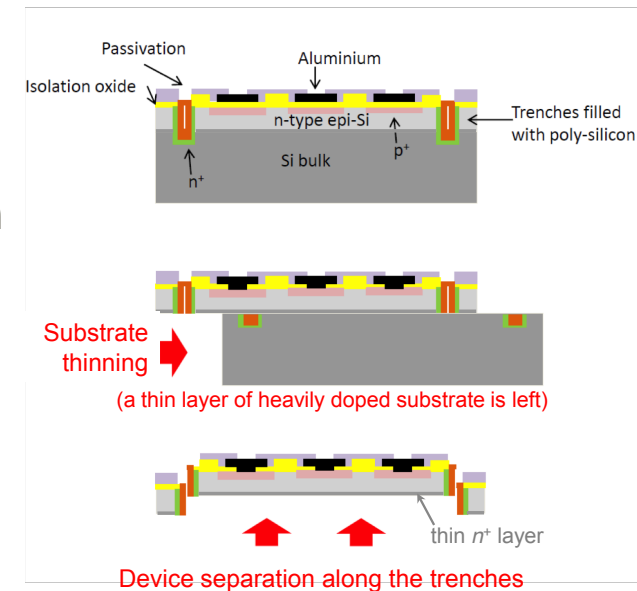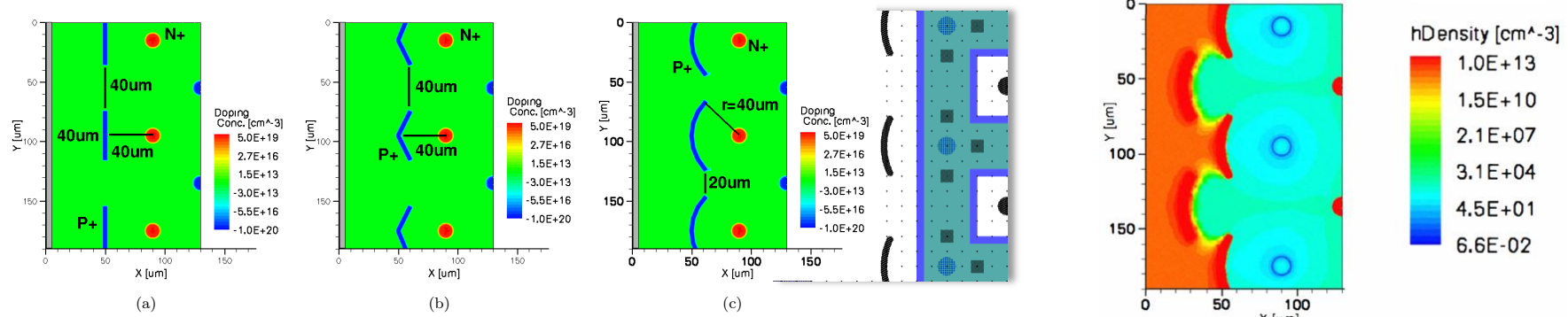
…nd Ac…

○ Ohmic (p+) electrodes

○ Mini…
active…

○ Trenches and implants "stop" the edge carrier far from active area
   ○ More efficient compared to passive Slim
   ○ Minimal distance from active area 40-50 µm

Simulation
Carrier concentration

3D device: thin active region

- Process optimization for thin sensitive volume (~150 μm)

- Today available thinning methods:
  - (1) Local thinning
  - (2) Bond wafer
  - (3) Optimized combination of (1) and (2)

- Technology compatible with 3D device processing
  - Single sided or Double sided 3D device process
  - Produced thin devices should be robust
    - Preferable 3D processing on thick wafer

  - Thinning method
    - (1) 3D Double sided process
    - (2) 3D Single sided process
   - (3) Robust as (2) with option of single/double sided process as (1)

Thin membrane

300um

Etched backside   500um
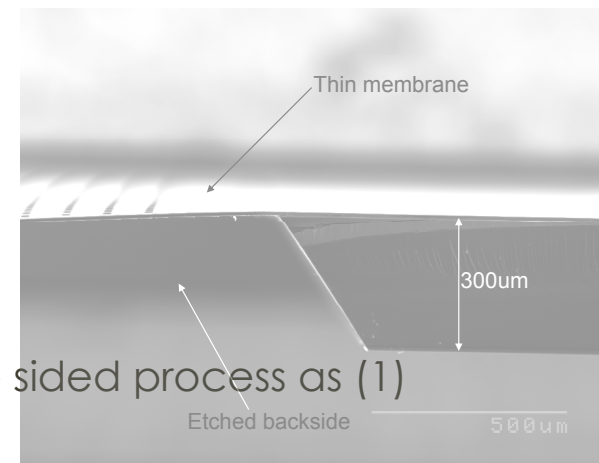
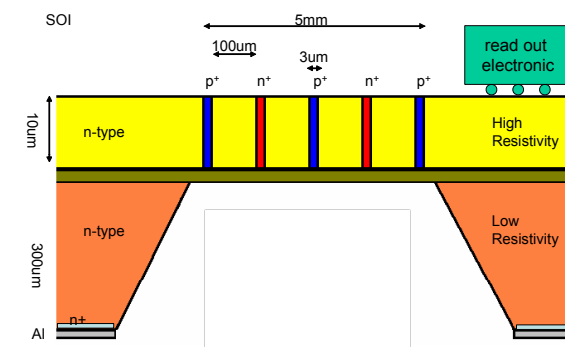- (1) Local thinning of sensor active areas with DRIE or TMAH

- Advantages: exploit the experience with double-sided process, sensor bias from the back-side, no support wafer (bonding and removal),
- Disadvantages: mechanical fragility, lithography on etched regions, active edge not feasible

- (2) Thin active volume on top of support wafer (wafer bond), thinner with Epi layer

SiO_2 →

| Sensor wafer |
| Support wafer |

E

P++
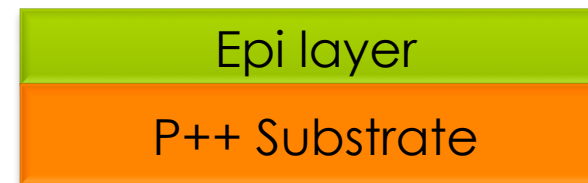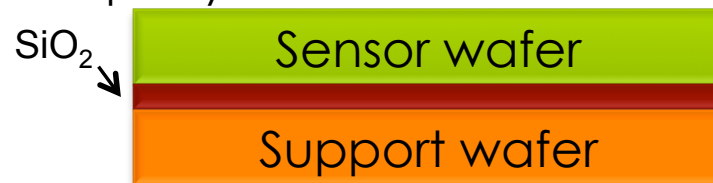
- Advantages: mechanical robustness, active edge feasible
- Disadvantages: support wafer (bonding and removal), bias from the front-side. Post processing for back-side bias: easier with Epi layer
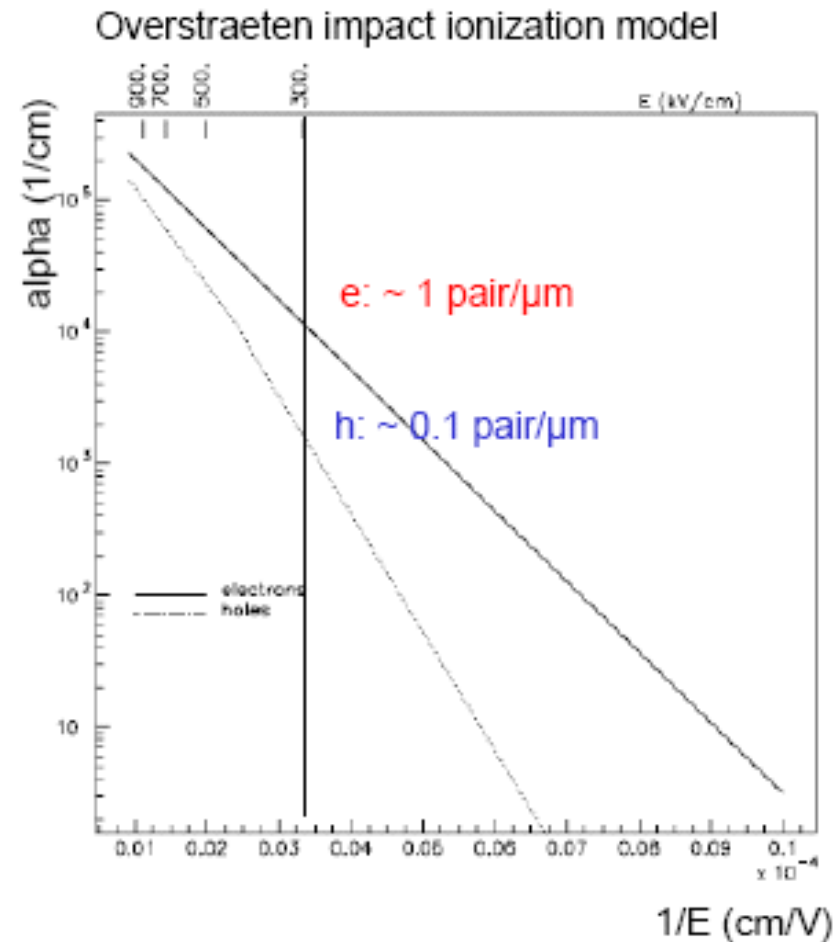
- (1) and (2) combined

SOI

5mm

100um   3um

read out electronic

p^+ n^+ p^+ n^+ p^+

10um   n-type   High Resistivity

300um   n-type   Low Resistivity

Al n^+

Thick silicon 300um thick

Thin silicon

Charge multiplication for thin bulk

- Charge multiplication in path length λ starts after a critical field value
  - e^- $V_{crit} \geq 300$ KV/cm
  - h $V_{crit} \geq 400$ KV/cm

$$N(\lambda) = N_0 \, e^{(\alpha \lambda)} = g \, N_0$$

$$N(\ell) = N_0 * \exp(\alpha * \ell) = g * N_0$$

- Near breakdown field value in silicon 300 kV/cm only e^- multiply
  - $\alpha_e \sim 0.7$ pair/µm
  - $\alpha_h \sim 0.2$ pair/µm

$$\alpha_{e,h}(E) = \frac{\alpha_e}{\alpha_h} = \alpha_{e,h}(\infty) * \exp\left(-\frac{b_{e,h}}{|E|} \right)$$

- Need to rise E-field as close to breakdown field as possible for high gain
  - prevent instability:
    - g ~10 for linear mode
      - $\lambda \sim 3$ µm near breakdown (collect e^-)

- Charge multiplication is always beneficial for particle tracking?
  - Excess of noise?
    - $ENC^2 = \ldots\ldots + A \, \tau \, 2 \, Q^2 \, F \, M^2 \, I_{det}$

      - F=1 for M=1 and F~2 for M>>1

Overstraeten impact ionization model

e: ~ 1 pair/µm

h: ~0.1 pair/µm

alpha (1/cm)

E (kV/cm)
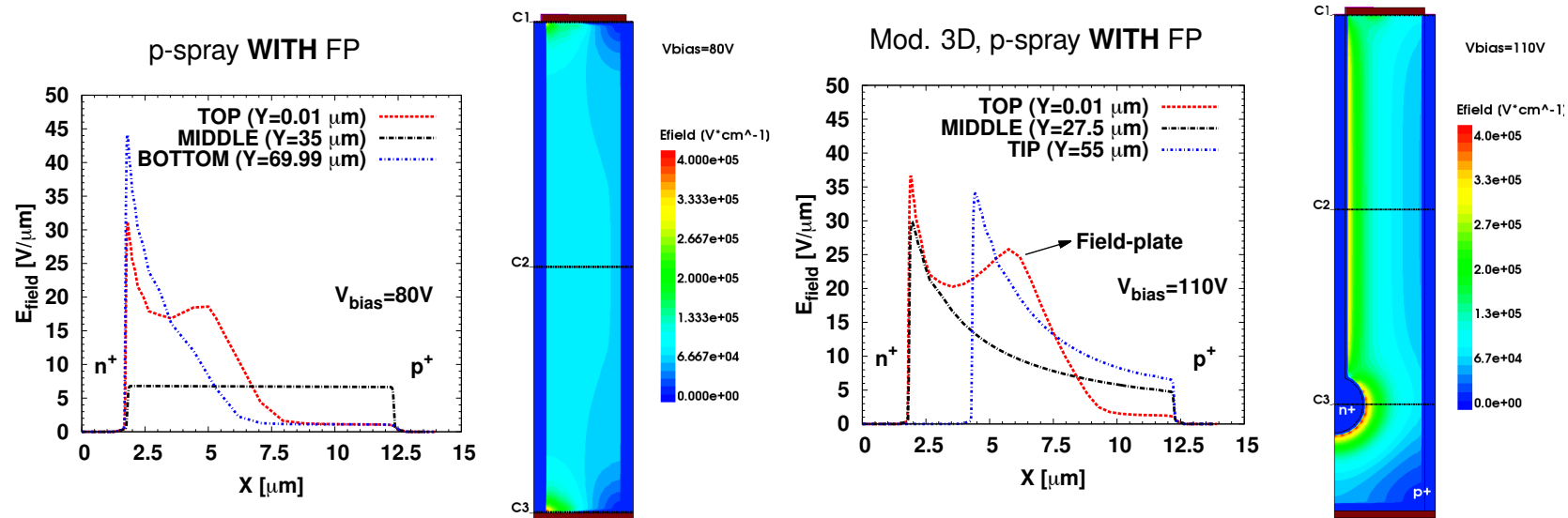
1/E (cm/V)

electrons
holes

[E. Gatti, P.M. Manfredi, Nuovo Cimento (1986), 9]
[V. Radeka, Ann. Rev. Nucl. Part. Sci. (1988), 38, 217]
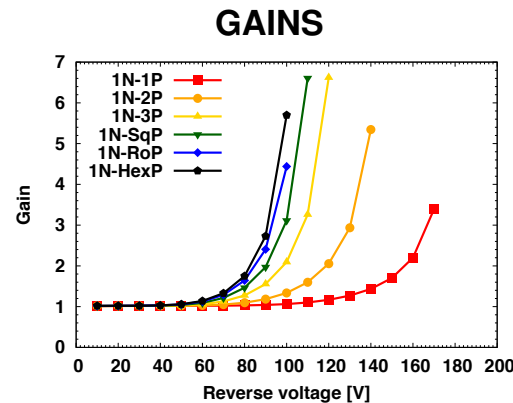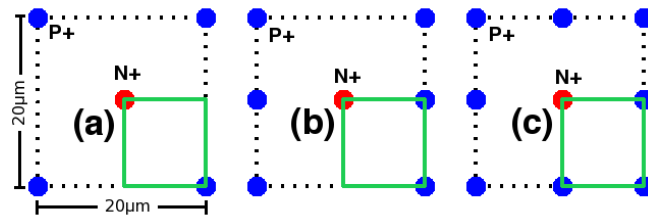
3D Charge multiplication

- New design of 3D devices, column:
  - High E-field at lower voltage: increase bulk and electrode doping
  - column geometry to decrease critical field regions
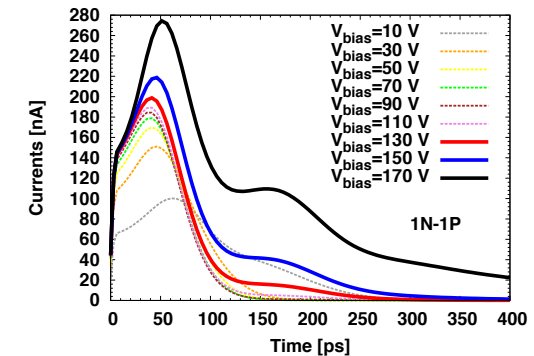   - Smaller radius to increase E-field
    - Tuned shape

p-spray **WITH** FP

Mod. 3D, p-spray **WITH** FP

3D Charge multiplication

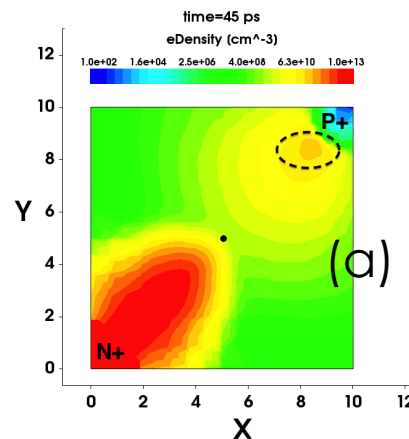○ New cell design for a "tuned low gain"

V_{bias} 130 V

GAINS

**Signal evolution (1N-1P)**

○ Time evolution of multiplied signal : m.i.p. going through the cell center

  ○ **(a)** e^- and **(b)** h 45 ns after the m.i.p. event;   **(c)** e^- and **(d)** h 175 ns after the m.i.p. event
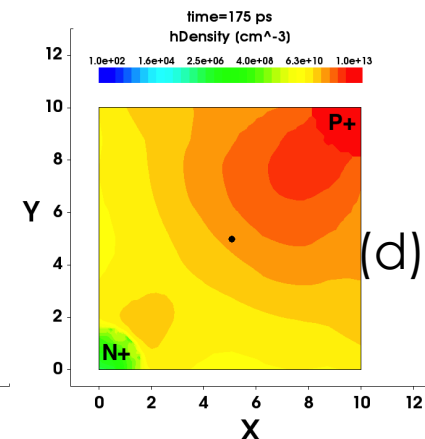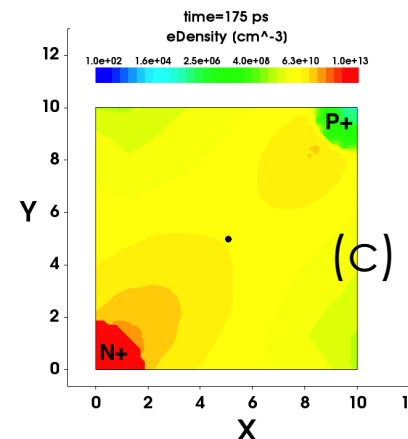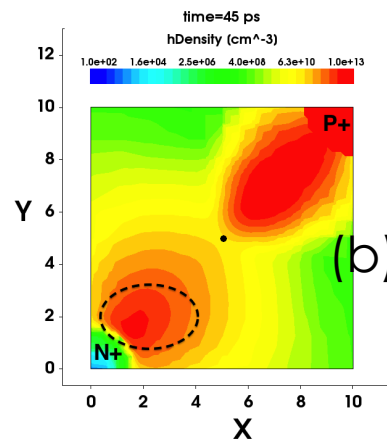
3D Charge multiplication: 4D Ultra-Fast Silicon detectors

- Exploiting the 3D charge multiplication R&D
  - Add a new functionality to 3D devices:
    - *Integrate to the optimal spatial resolution of Pixel detectors the 4th coordinate, namely "time" T*
      - Goal is to design devices with T resolution in the range of a few tens of ps

  - Simulation results support the feasibility of 3D-4D devices
    - **Intrinsically fast 3D detectors with optimized time resolution**
      - **Rise time of the faster signals ~ 50 ps.**

Signal evolution (1N-1P)

- In order to be "time tagger" a device should
  - Collect the faster carrier
  - Have short charge collection distance
  - Optimized E-field
  - Maintain signal efficiency
  - Novel R&D on going for Planar and 3D devices
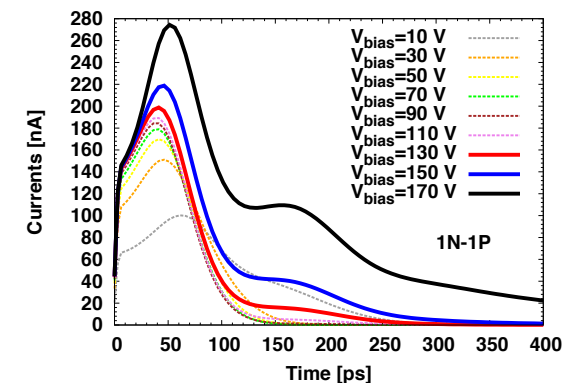
Examples and exercises

- Seems that increasing electrode density is a beneficial strategy.
  - Discuss if for a hybrid pixel 3D detector with pitch size smaller than ROC size, more readout electrodes per pixel, could be drawbacks.

- Design the geometry of a 4D pixel detector
  - Compare Planar with 3D design
    - Consider: bulk thickness, load C, signal size and "real" signal threshold, S/N, safe multiplication gain, collection time, ...
      - Compare performance for the two solutions

THE END

Suggested Papers and Books

- S. M. Sze: Semiconductor Devices, Physics and Technology, Wiley 1985
- R. S. Muller, T. I. Kamins: Device Electronics for Integrated Circuits, John Wiley & Sons 2003
- H. Spieler: Semiconductor Detector Systems, Oxford University Press, 2005
  - Spieler ha anche molti tutorials utilissimi
    - http://www-physics.lbl.gov/~spieler/

- Rossi, Fischer, Rohe, Wermes: Pixel Detectors: from Fundamentals to Applications, Springer 2006
- G.Lutz : Semiconductor radiation detectors, Device Physics, Springer 1999

Papers & PhD thesis & Workshops

- IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 55, NO. 5, OCTOBER 2008, 2775
- Nuclear Instruments and Methods in Physics Research A 587 (2008) 243–249
- Nuclear Instruments and Methods in Physics Research A 694 (2012) 321–330
- IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 48, NO. 5, OCTOBER 2001
- Nuclear Instruments and Methods in Physics Research A 501 (2003) 138–145
- Nuclear Instruments and Methods in Physics Research A 509 (2003) 86–91
- Nuclear Instruments and Methods in Physics Research A 560 (2006) 127–130
- Nuclear Instruments and Methods in Physics Research A 650 (2011) 150–157
- Nuclear Instruments and Methods in Physics Research A 549 (2005) 122–125
- Nuclear Instruments and Methods in Physics Research A 638 (2011) 33–40
- Nuclear Instruments and Methods in Physics Research A 659 (2011) 272–281
- 2009 JINST 4 P03010 (http://iopscience.iop.org/1748-0221/4/03/P03010)
- Nuclear Instruments and Methods in Physics Research A 579 (2007) 642–647

- Link to interesting workshops
  - http://rd50.web.cern.ch/rd50/
  - http://tredi2013.fbk.eu/
- PhD thesis
  - Angela Kok, BRUNEL UNIVERSITY
  - M. Povoli, DISI - University of Trento
  - G. Douglas Stewart, University of Glasgow
  - D. Bassignana, Universidad Autonoma de Barcelona

EXTRA

o Column capacitance

Thi k   d fl
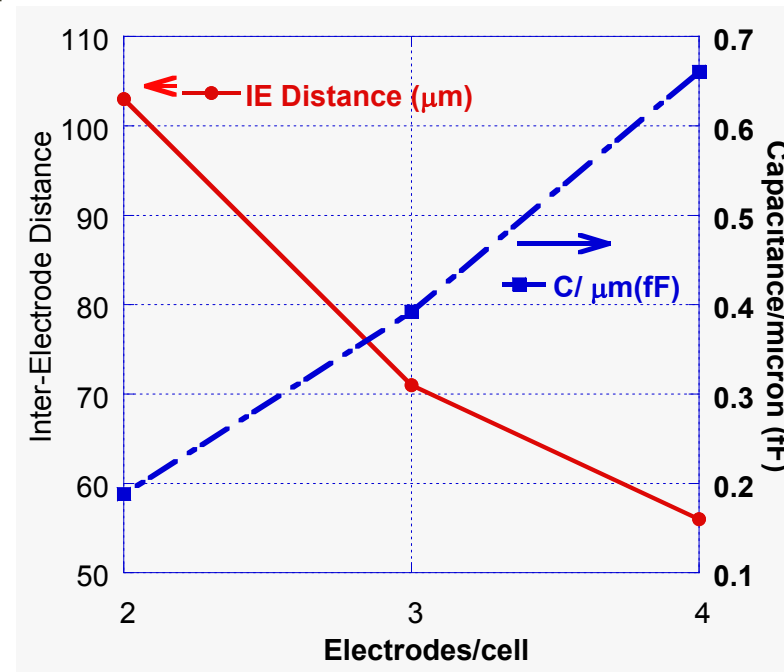
Can 4D-UFSD work? Correct Collected Charge

Collection time = thickness/v_{sat} (v_{sat} = 80 μm/ns) (holes)

Realistic gain & ca

Thickness	BackPlane Capacitance		Signal	Coll. Time	Gain required	
[um]	Pixels [fF]	Strips [pF/mm]	[# of e-]	[ps]	for 2000 e	for 12000 e
1	**250**	5.0	35	13	57	343
2	125	2.5	80	25	25	149
5	50	1.0	235	63	8.5	51
10	25	0.50	523	125	3.8	23
20	13	0.25	1149	250	1.7	10.4
100	3	0.05	6954	1250	0.29	1.7
300	1	0.02	23334	3750	0.09	0.5

Good time resolution

For pixel thickness > 5 um, Capacitance to the backplane C_b < C_{int} (200 fF)

For pixel thickness = 2 um, C_b ~ ½ of C_{int}, and we might need bipolar (SiGe)?

Viable sensor thickness 2 μm – 10 μm (i.e. 20-100ps)

Needed Gain: Pixels 4 – 25, Strips (1 mm) 20- 150

(much less than APD's or SiPM)

Note: CNM (Barcelona) is routinely producing 10 μm thick sensors.

6

dc

Method -- SCP Treatment

SCIPP

Scribing

finished die

Cleaving

finished die

Passivation

finished die with slim edge

FONDAZIONE
BRUNO KESSLER
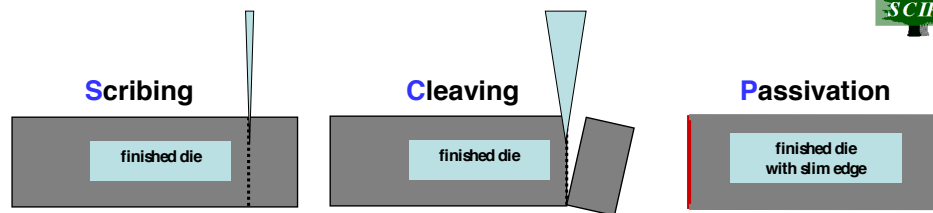
Native Oxide
+ Radiation
or:

N-type   P-type

➢ Native SiO_2 ➢ ALD
  + UV light   of Al_2O_3
  or high T
➢ PECVD SiO_2
➢ PECVD Si_3N_4
➢ ALD "nanostack"
  of SiO_2 and Al_2O_3

Key steps of the Active-Edge technique on EPI wafer:

- Trench etching by DRIE :
  ≈ 5 µm wide,
  ≥ 50 µm deeper than EPI thickness.

- Trench filling with polysilicon, to allow for subsequent litho steps;
  the deposited poly thickness is about half the trench width.

- Deep into the trench, a narrow unfilled gap remains, which allows separating the devices along the trench after the substrate is thinned down.

- A thin layer of heavily doped substrate is left, acting as an ohmic backside contact.

- If required for the bias contact, the device can finally be metallized on backside.

Passivation

Aluminium

Isolation oxide

n-type epi-Si

p^+

Trenches filled with poly-silicon

Si bulk

n^+

Substrate thinning

(a thin layer of heavily doped substrate is left)

thin n^+ layer

Device separation along the trenches
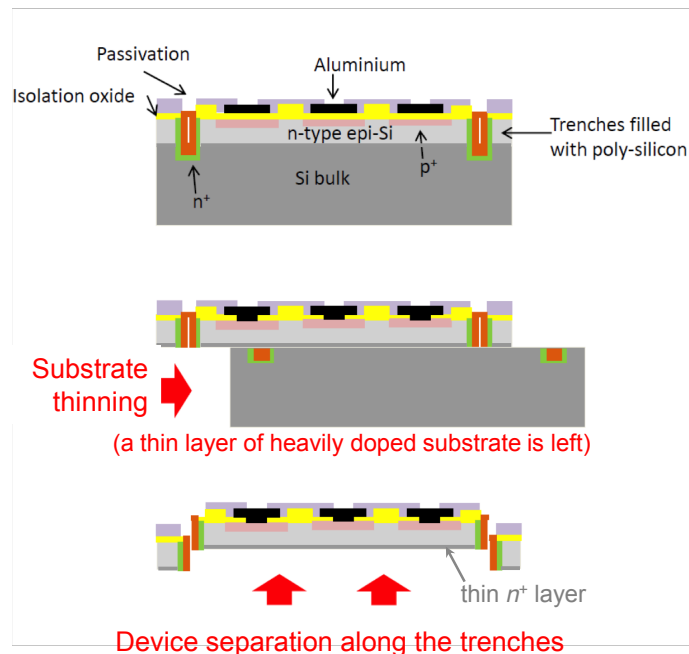
DRIE for Through Silicon Vias [4]

- Holes are formed by rapidly alternating etches with SF_6 and passivation with C_4F_8

- Any size hole is possible (0.1 -800 um)

- Etch rate is sensitive to hole depth and AR (aspect ratio).

Bosch Process Principle

F + ions   SiF$_4$ Mask

Si   SF$_6$ Plasma

-CF$_2$-

Si   C$_4$F$_8$ Plasma

Thin fluoro-carbon polymer film (passivation)

Scalloping   SF$_6$ Plasma

Ray Yarema   Vertex 2010
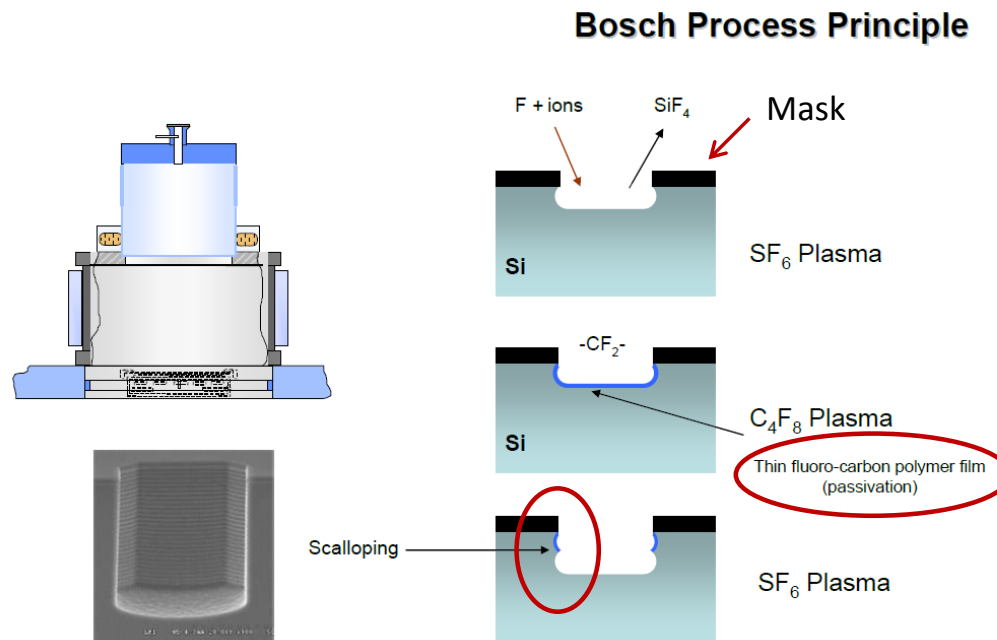
D- RIE

Deep reactive-ion etching (DRIE) is a highly anisotropic etch process

Aspect ratio of 20:1 or more.

The Bosch process alternates repeatedly between two modes to achieve nearly vertical structures.

1. A standard, nearly isotropic plasma etch SF_6

2. Deposition of a chemically inert passivation layer C_4F_8
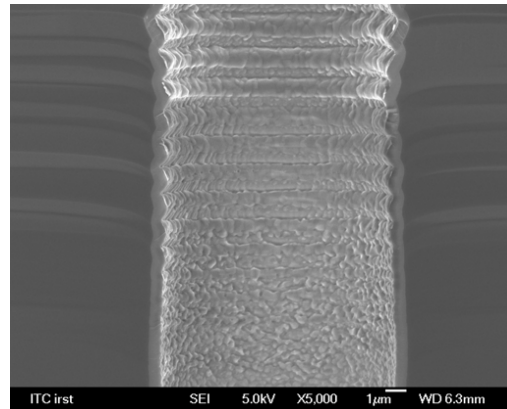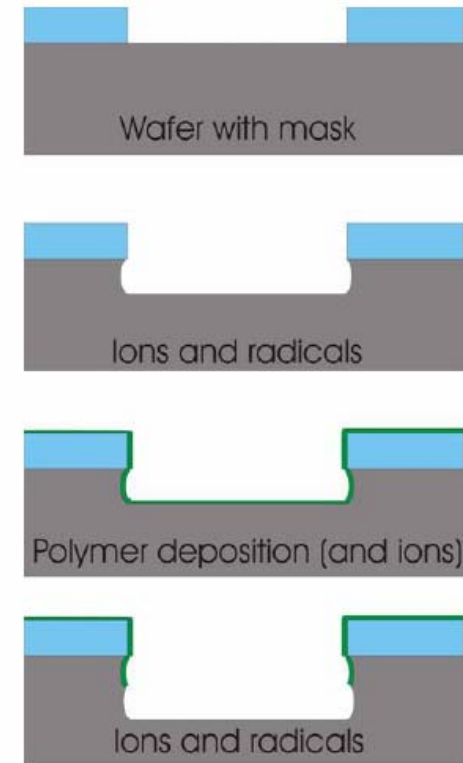
Legnaro 2007   Maurizio Boscardin

3D fabrication processes
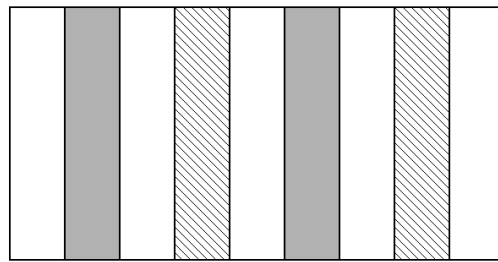
Stanford (SNF), SINTEF

(a)
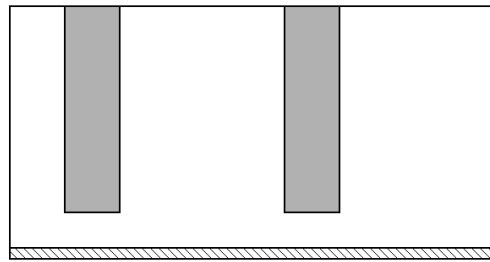
FBK, VTT

(b)
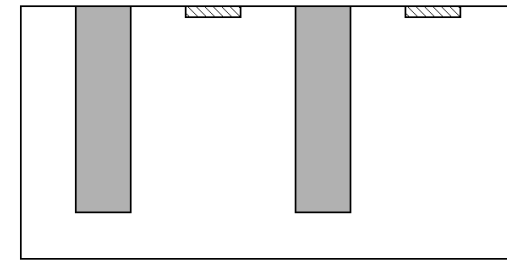
BNL

(c)
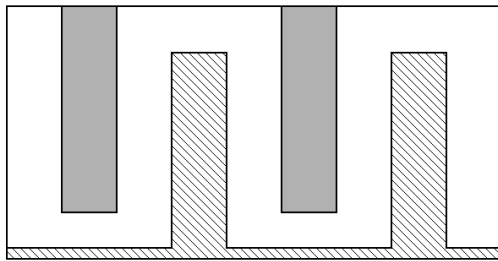
FBK

(d)
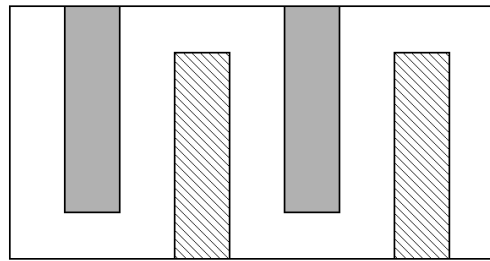
CNM

(e)
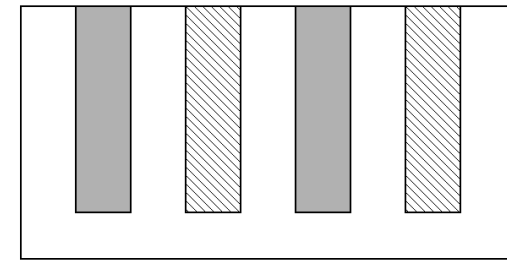
BNL

(f)

Figure 3.14: Schematic representations of all the proposed approaches to the 3D technology: the original architecture (a) is compared with: Single Type Column implementations from FBK/VTT (b) and BNL (c), Double Sided Double Type Columns from FBK (d) and from CNM (e) and finally the single sided double type column from BNL (e).

Reasons for dead borders on standard planar technology sensors
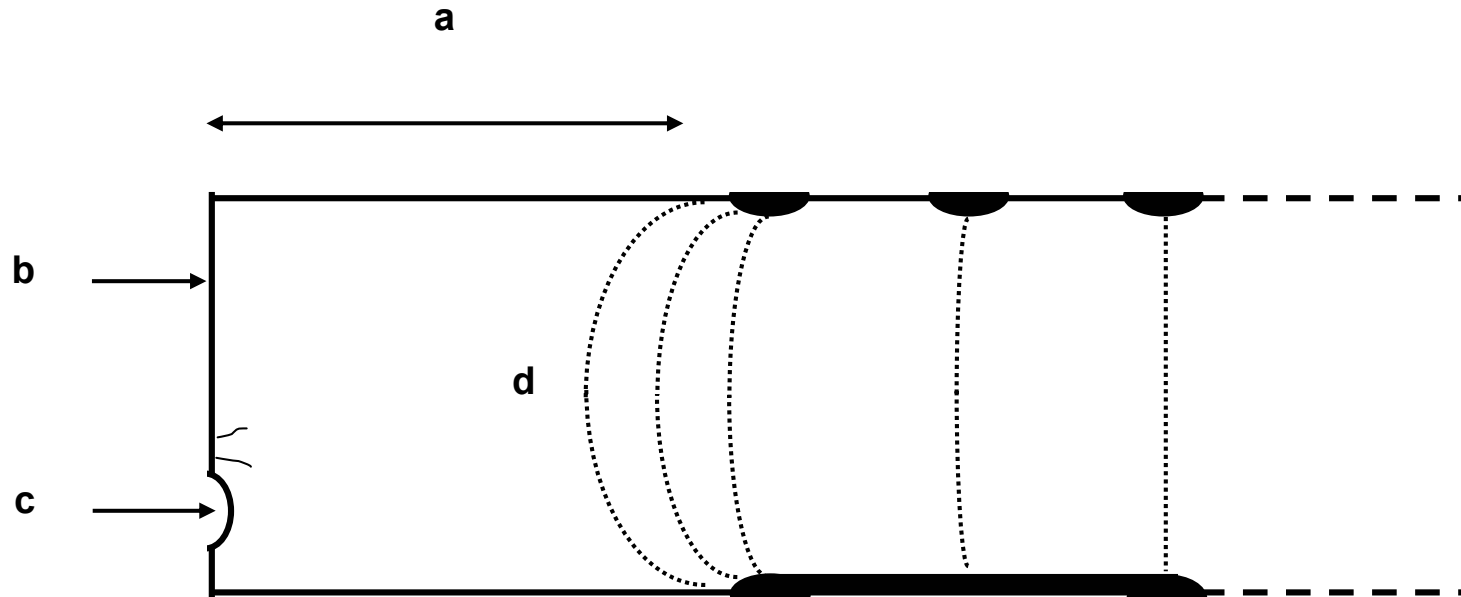
a. space for guard rings
b. sawed edges connecting top and bottom are conductors
c. chips and cracks are also conducting and can reach inside the edges
d. the field lines bulge out, and should be kept away from b and cs

3D edge sensitivity using 13 keV X-rays at Berkeley

X-ray

Cinzia Da Vià - Vertex 06 - Perugia - September 2006

30 Volts

■	45-54
■	36-45
□	27-36
□	18-27
■	9-18
□	0-9

10-90% < 5μm
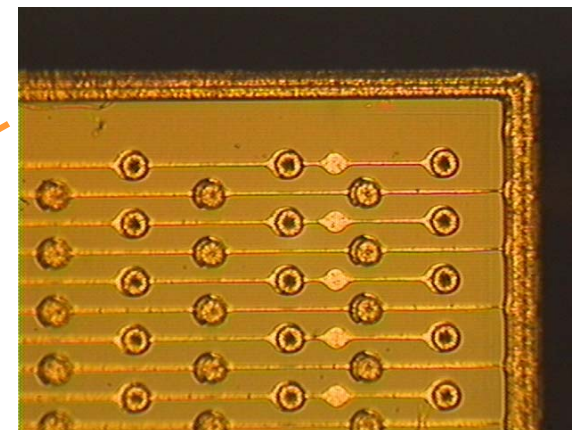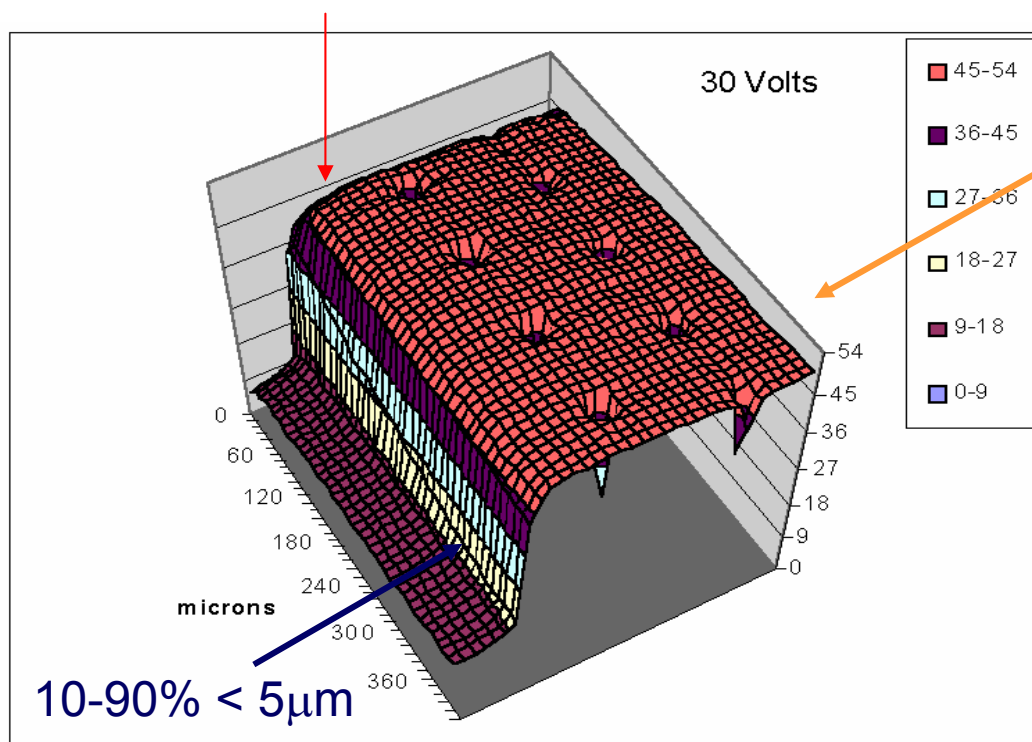
Measurement
Performed using a
2 μm beam

J. Hasi, C. Kenney,
J. Morse, S. Parker

Electrodes ~ 1.8% of total area

X-ray micro-beam scan, in 2 μm steps, of a 3D, n bulk and edges,
181 μm thick sensor. The left electrodes are p-type
Efficiency measured in test beam ~98%

Legnaro 2007   Maurizio Boscardin

Efficiency: p and n electrodes response
Electrodes area ~1.8% of total area

A. Kok PhD thesis

Cinzia Da Via'- Vertex 06 - Perugia - September 2006

Cell study using 120GeV muons (Cern X5), Telescope Precision ~4μm.

Electrode response using 12KeV X-ray beam (ALS), beam size ~ 2μm

50μm

100μm

n

p

n

n

n

n

Detector 1 & 3 Cell Efficiency Map

X-Projection
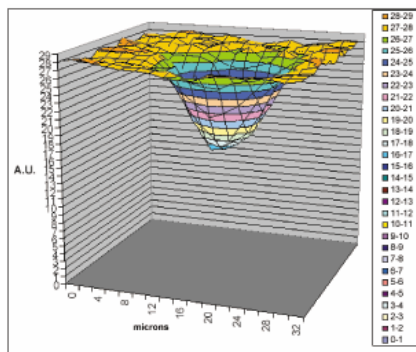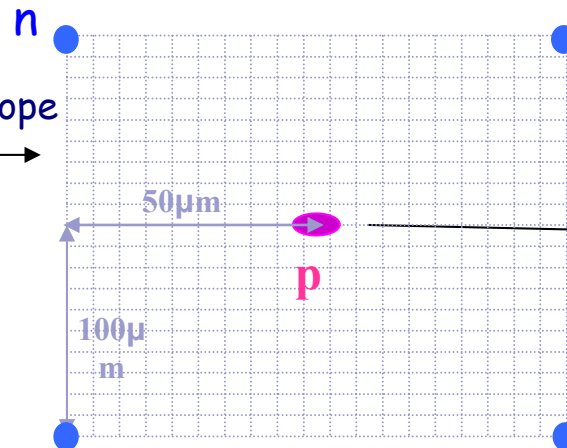
N – Electrode

Signal Reduction 43%
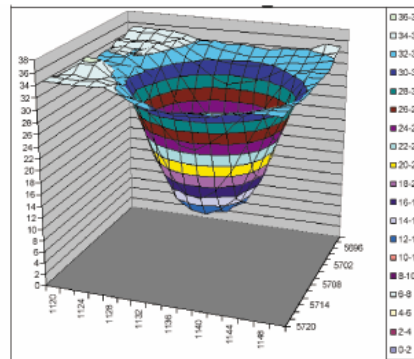
P – Electrode

Signal Reduction 66%

Differences between N and P:

Grain size of poly, Diameter, Diffusion rate, Trapping, Doping
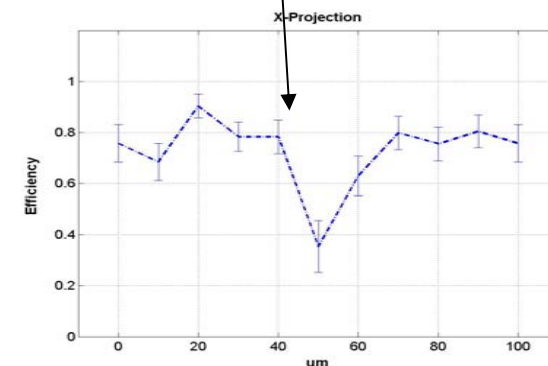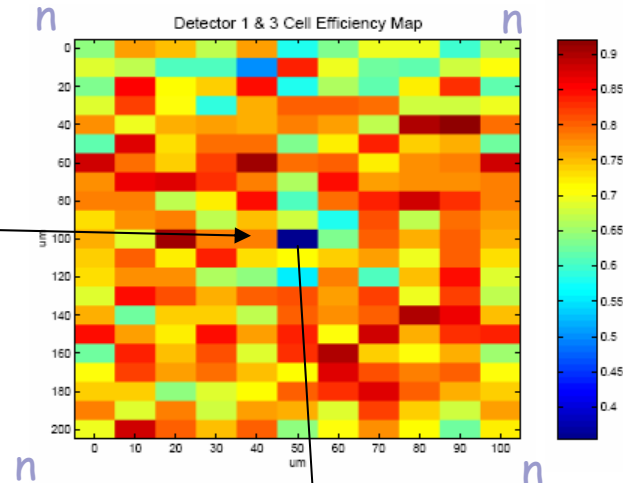
40% reduction in count efficiency at p-electrode

J. Hasi, PhD thesis

Legnaro 2007

Maurizio Boscardin

New technology
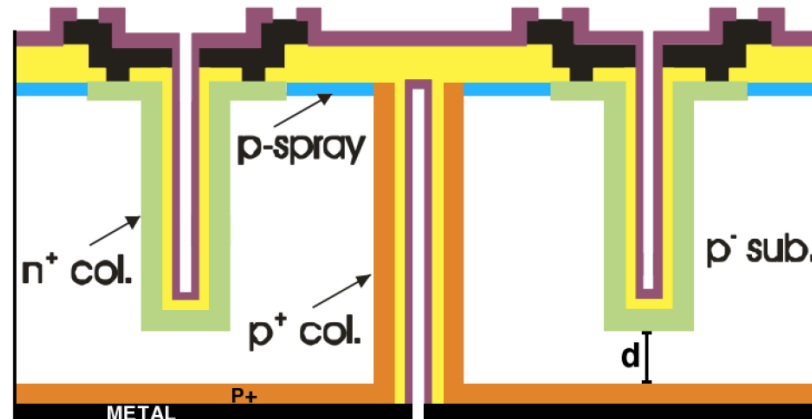
- partially etched junction columns;
- passing-through ohmic columns for effective slim edges
- reduction of back-side masks;
- process simplification.

optimization of the DRIE step to accurately control columns depth
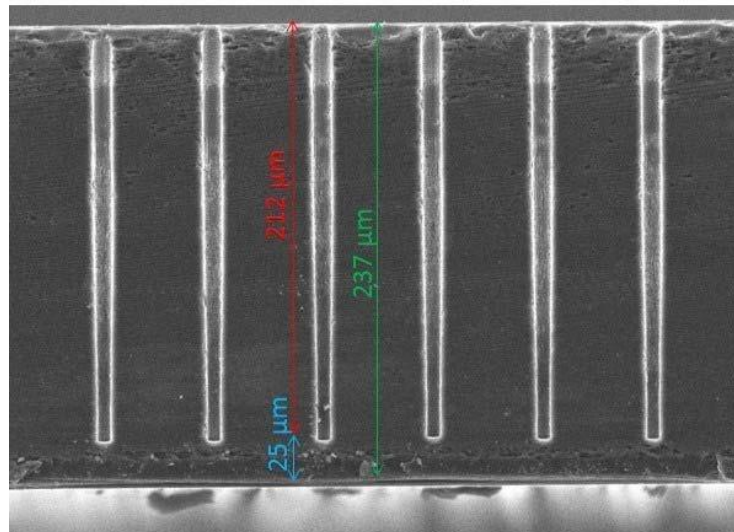
breakdown simulation: 20 to 100V improvement
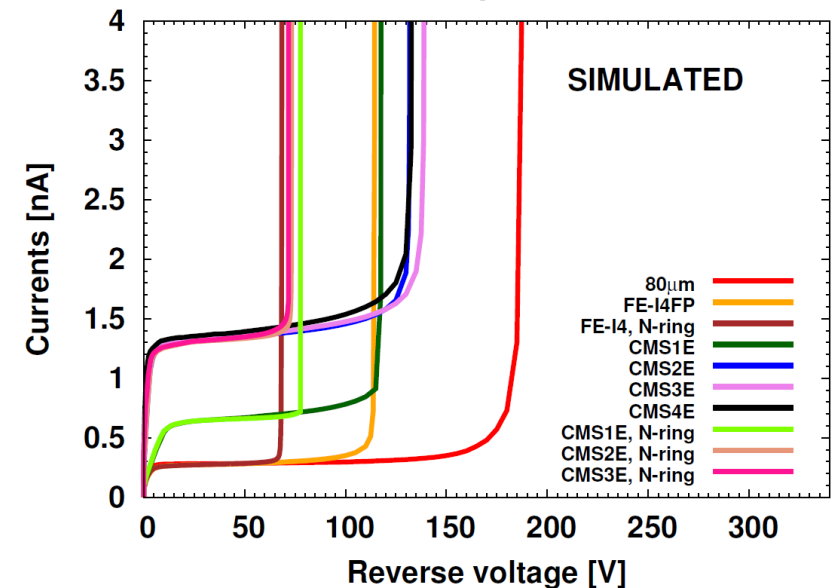
Optimize edge protection: wafer bowing

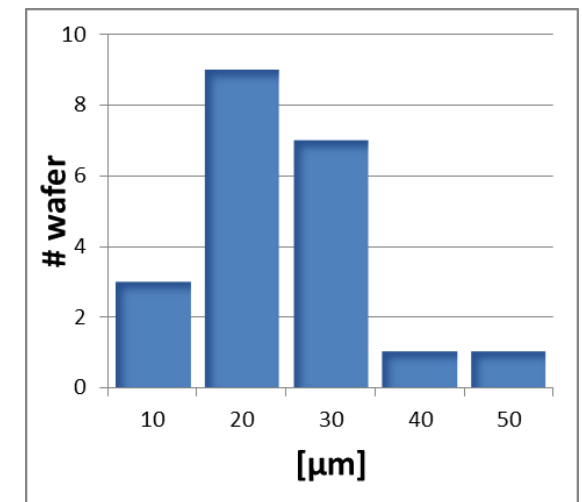Edge protection effects on the wafer bowing.

A high bowing induces →
- High leakage current
- Misalignment among columns
- Bonding problem
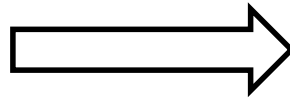
Old edge protection → wafers warp up to 120 μm

Optimized edge protection → wafers warp < 30 μm
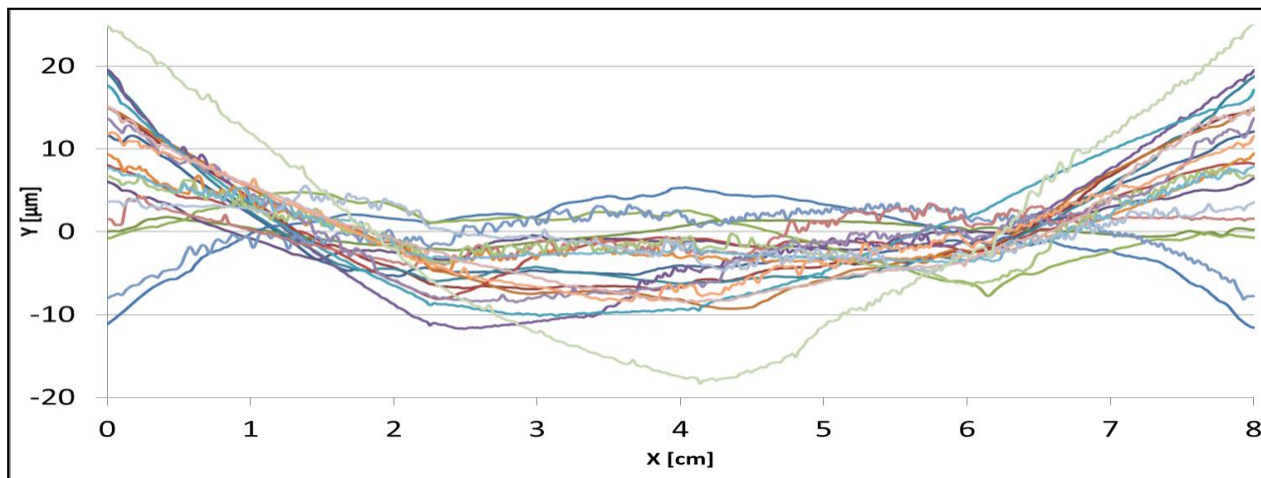
3D_ATLAS10

TRAPPING in Si → COLLECT ELECTRONS, INCREASE E-field

and USE SHORT 'IES' (THIN SUBSTRATES FOR PLANAR) NIMA 603 (2009) 319–324

Cinzia Da Viá, Uni. Manchester, Trento Workshop 20th February 2013
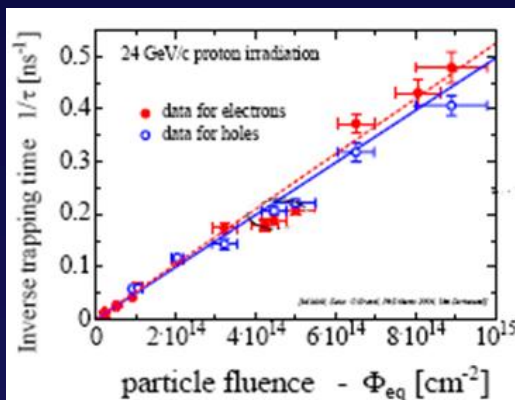
$$\tau_{tr}$$
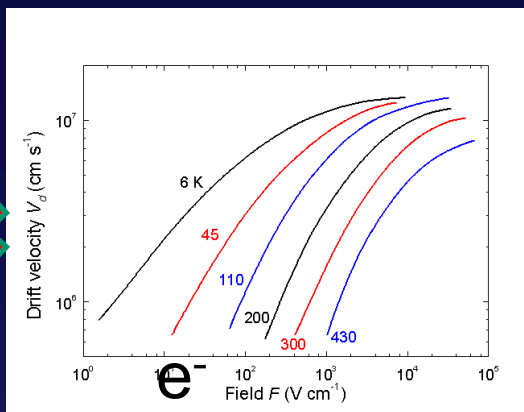
$$V_{drift}$$
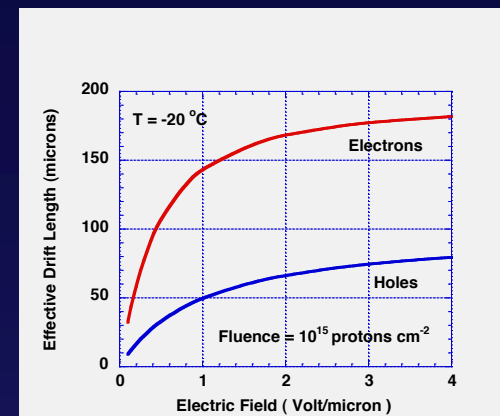
$$\lambda \quad \text{(trapping distance)}$$

$$\frac{dS}{dt} = q \frac{dV_W}{dx} \frac{dx}{dt} \exp\left(-\frac{x}{\lambda}\right)$$

$$S = \frac{\lambda}{L}\left[1 - \exp\left(-\frac{x}{\lambda}\right)\right]$$

Expected signal
After irradiation
Without multiplication
Depends on λ/L
This is also true for
diamond

Trapping times from Kramberger et al.
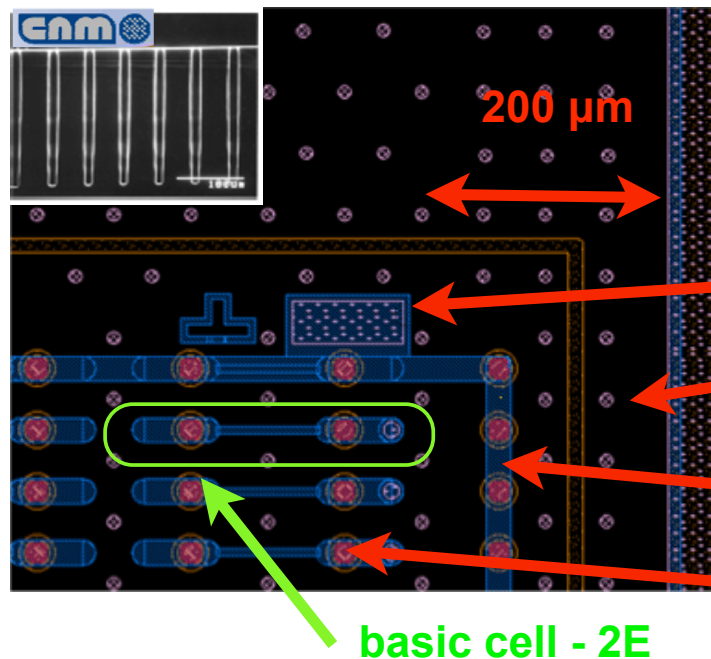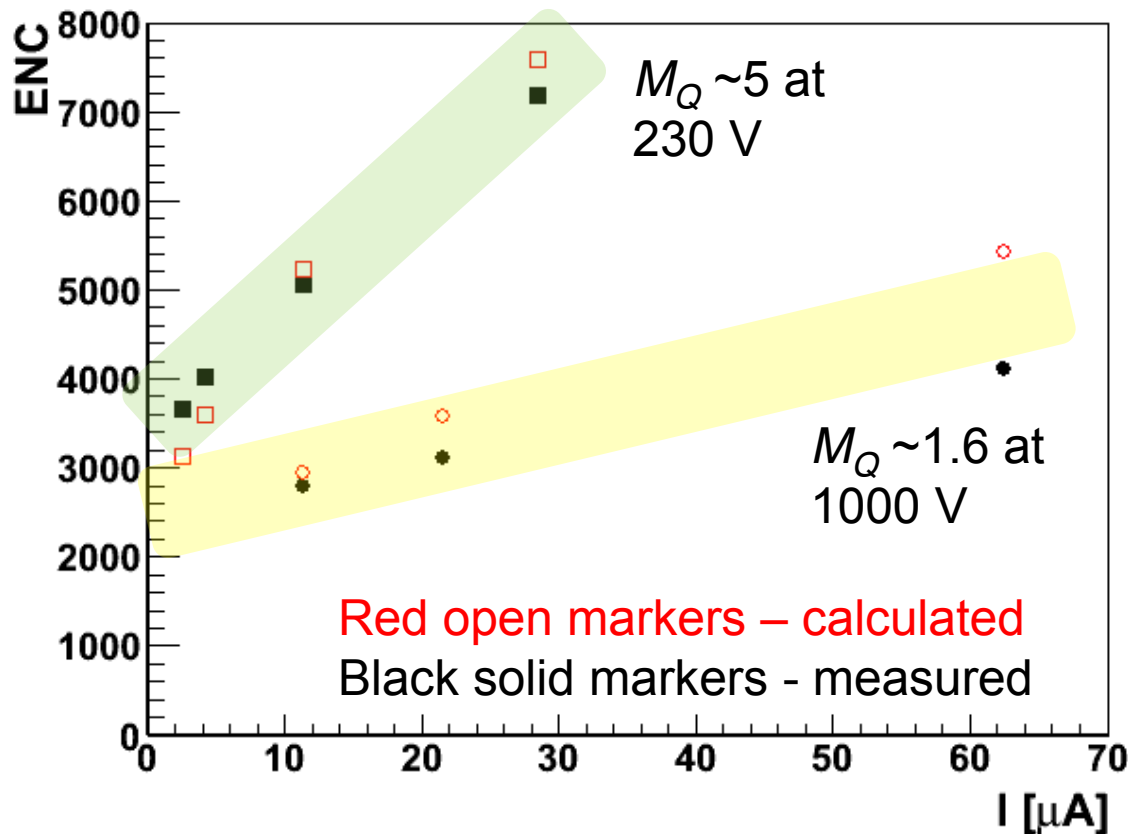NIMA 481 (2002) 100
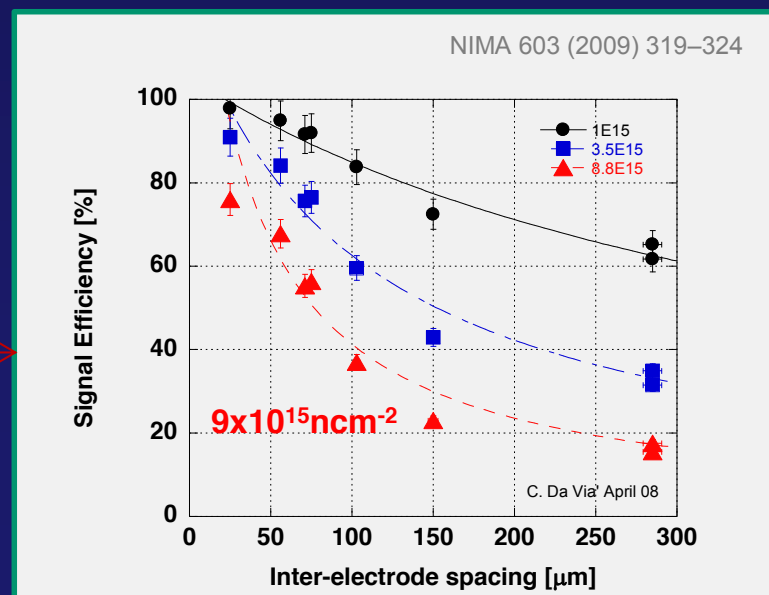
3D IBL Production
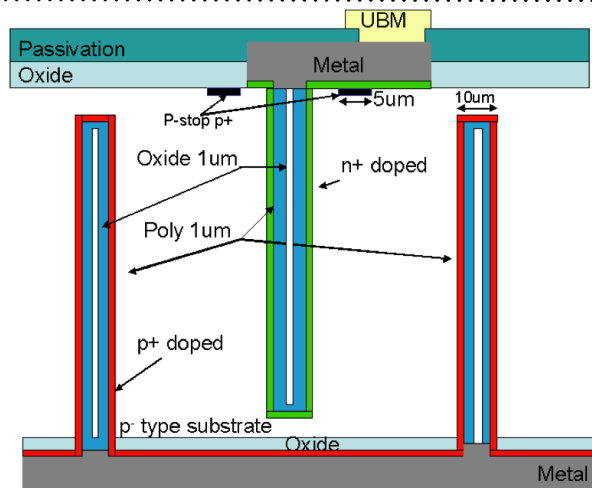
- **Main 3D-CNM features:**
  - **D**ouble-side **D**ouble **T**ype **C**olumns (DDTC) process
  - no supporting wafer
  - isolation: p-stop
  - sensor thickness *230 µm*
  - no full 3D: columns deepness *210 µm*
  - column diameter *10 µm*
  - columns filled with polysilicon
  - 3D guard ring + fences (*200 µm*):
  - Front End: FE-I4 readout chip
  - More Radiation Hardness: needs ~*150V* vs 1000V (planar) to achieve hit efficiency >98% ($5 \times 10^{15} n_{eq}/cm^2$)

200 µm

Probe for quality assurance

p+ implant (fences)

3D guard ring

n+ electrode (readout)

basic cell - 2E

FE-I3

FE-I4

A. Micelli

3

Trento, Feb 19 2013
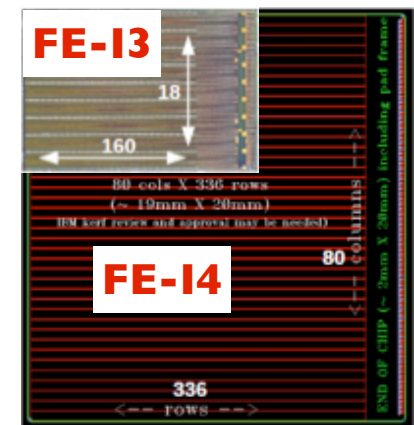
Calculation of the noise

$M_Q \sim 5$ at 230 V

$M_Q \sim 1.6$ at 1000 V

Red open markers – calculated
Black solid markers - measured

$$ENC^2 = ENC_{MI}^2 + ENC_S^2$$

$ENC_S = 2300$ e – series noise

$$ENC_{MI} = MI \cdot \sqrt{F} \cdot ENC_I$$

$$ENC_I = e/2 \cdot \sqrt{I_{gen} e_0 \tau}$$

ENC_I –noise due to generation current without amplification – short noise (CR-RC shaping)
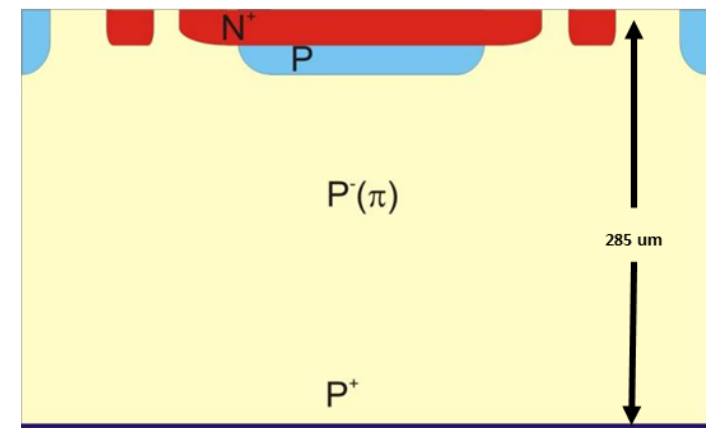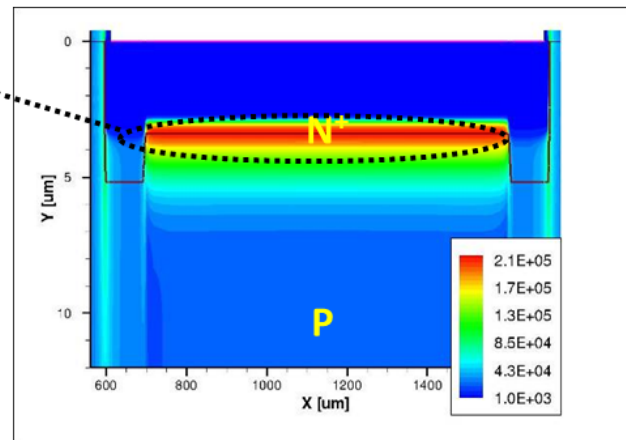
$F = 2$ for $M \gg 1$, $F=1$ for $M \sim 1$

$\tau = 25$ ns

$I_{gen} = \alpha \cdot \Phi_{eq}$ $M_I \sim M_Q$

Good agreement between measured and calculated noise.

Creating a n++/p+/p- junction along the centre of the electrodes. Under reverse bias conditions, a high electric field region is created at this localised region, which can lead to a multiplication mechanism[2].

_____

[2]P. Fernandez et al, "Simulation of new p-type strip detectors with trench to enhance the charge multiplication effect in the n-type electrodes", Nuclear Instruments and Methods in Physics Research A658 (2011) 98–102.

Optimize edge protection

Table 4
Summary of the yield on selected wafers from the first productions batches.

Batch	Total wafers	Total sensors	Good sensors	Yield (%)
FBK-A10	12	96	58	60.4
FBK-A11(*)	4	32	14	43.7
CNM1	18	144	86	59.7
CNM2	15	120	85	70.8
Total	49	392	243	62.0

Mechanical fragility of wafers manly due to a cracks on the wafer edge caused by D-RIE etch step:
  ✓ Need a special edge protection during DRIE etching (electrostatic clamping) to prevent the creation of cracks that could cause the breakage during the processing.
  ✓ Need a special care during processing

Mechanical yield with the optimized edge protection:

	initial wafers	broken wafers	mechanical yield (%)
3D ATLAS 10	25	5	80%
3D ATLAS 11	25	3	88%
3D ATLAS 12	23	6	74%
3D ATLAS 13	20	8	60%

MicroTechnologies Laboratory
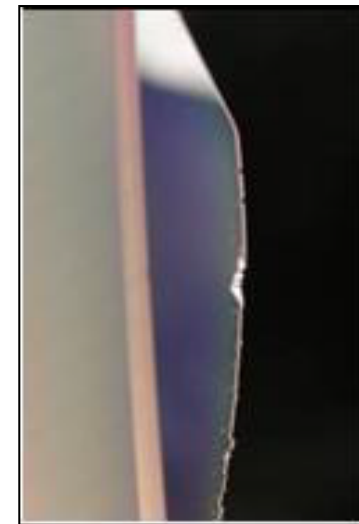
Wafer bowing: leakage current

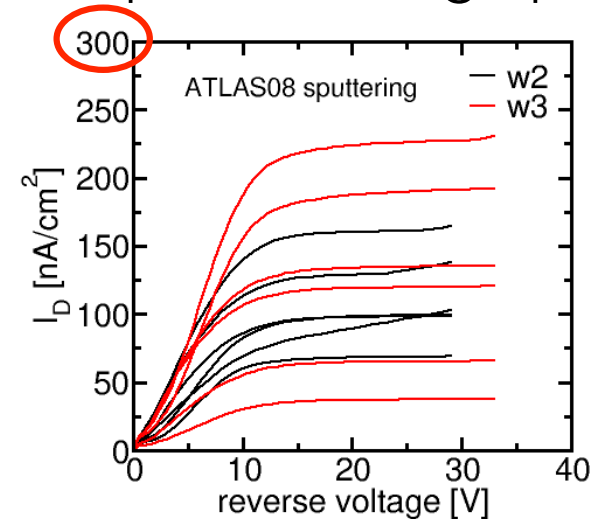The wafer bowing strongly influences the leakage current.

With the optimized edge protection it is reduced of one order of magnitude.

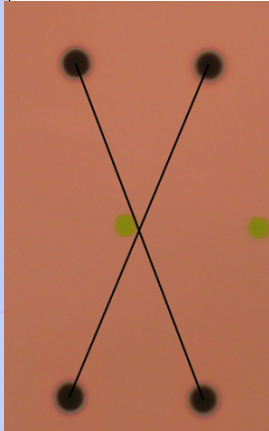Leakage current on planar test diodes (4mm^2)
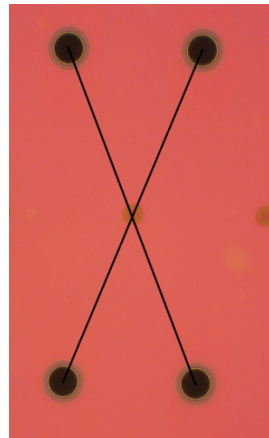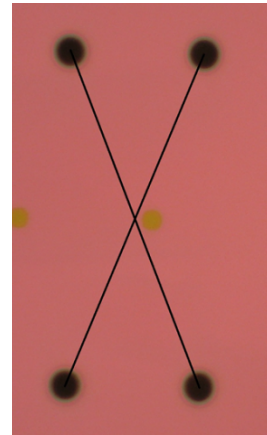
Old edge protection
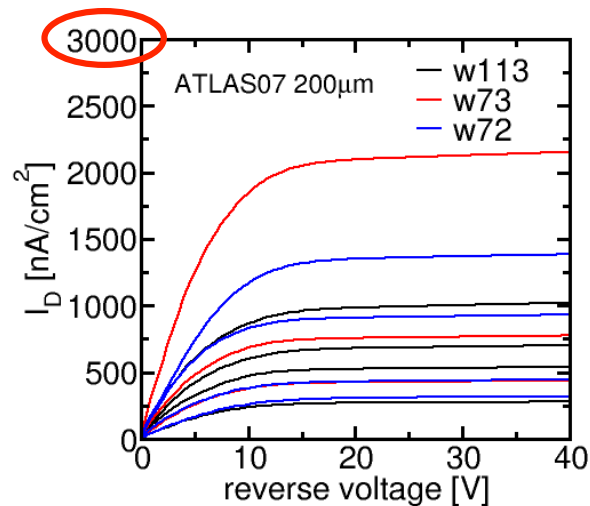
Optimized edge protection

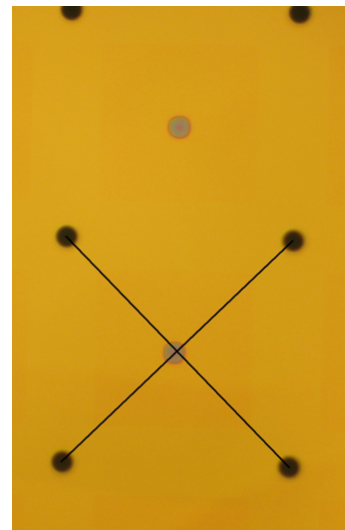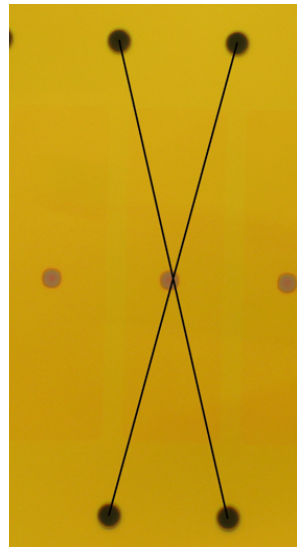# *Wafer bowing: Column alignment*

left side   center   right side

old edge protection
misalignment of a several μm
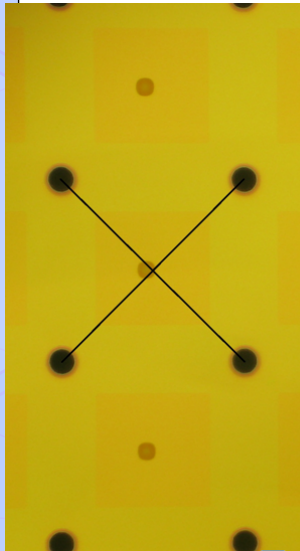
optimized edge protection layer

Misalignment < 5µm

MTLab
MicroTechnologies Laboratory

Signal Efficiency and Signal Charge in 3D structures

3D

particle

n+   p+   n+   p+   n+   p+   n+   p+   n+

L   Δ

~50 μm

Active edge ~4μm

~ 500 μm

L=Δ

i

n+

PLANAR
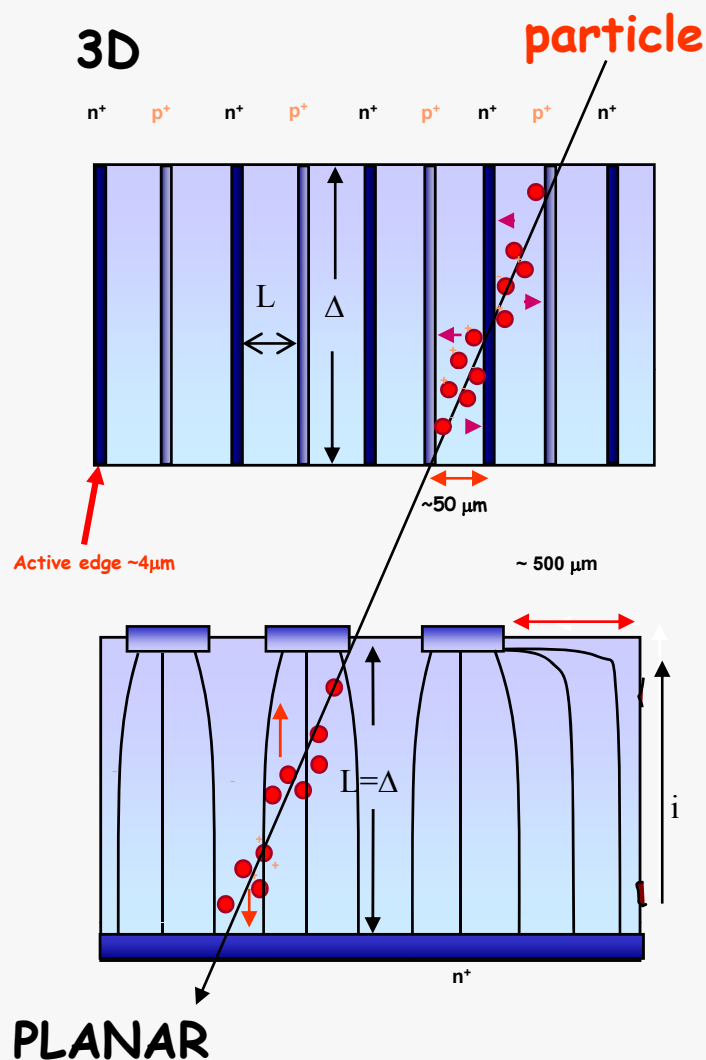
$$\frac{dS}{dt} = q \frac{dV_W}{dx} \frac{dx}{dt} \exp(-\frac{x}{\lambda})$$

$$S = \frac{\lambda}{L}\left[1 - \exp(-\frac{x}{\lambda})\right]$$

$$SE = \frac{\lambda}{L} - \left(\frac{\lambda}{L}\right)^2 + \left(\frac{\lambda}{L}\right)^2 \exp(-\frac{L}{\lambda})$$
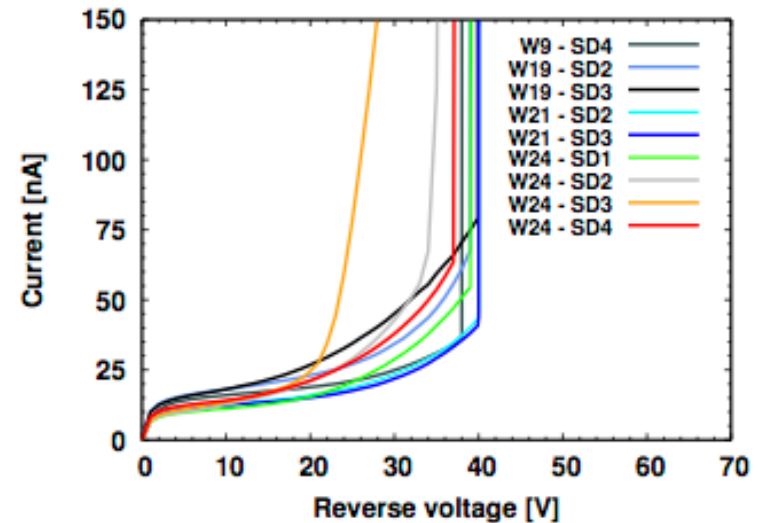
$$SE = \frac{1}{1 + 0.6L \dfrac{K_\tau}{v_D} \Phi}$$
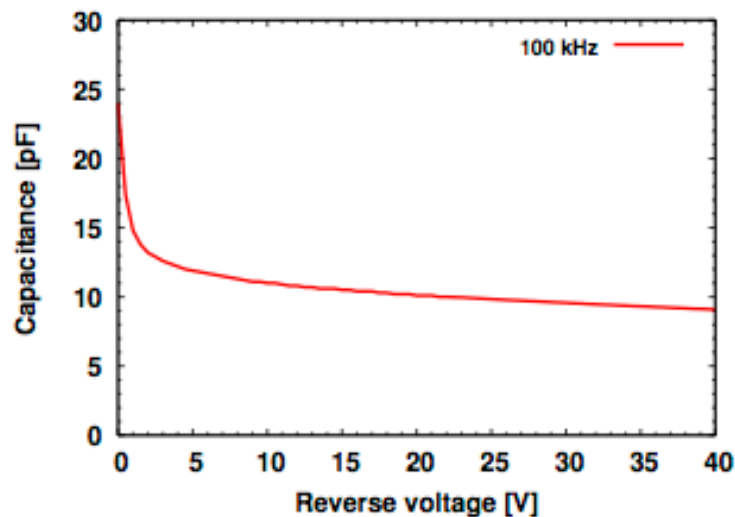
L=Inter electrode distance
Δ=thickness

Trapping times from Kramberger et al.
NIMA 481 (2002) 100
NIM A 501(2003) 138 (Vertex 2001)

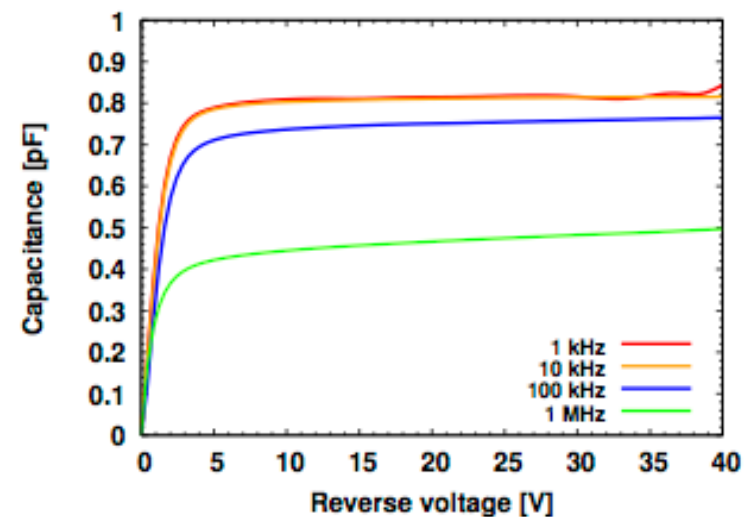# Electrical Characterization: IV, CV

- Good leakage current with breakdown at about 40 V

- Strip to backplane capacitance indicates full depletion is reached at about 5 V

- Inter-strip capacitance is less than 1 pF

Strip to back capacitance

Inter-strip capacitance

- As can be seen in Fig.3, interpixel capacitance (i.e. the capacitance between the junction (n) columns of the adjacent pixels) is negligible, because of the shielding action of the ohmic-p-columns. On the other hand, the backside capacitance (i.e. the capacitance between the n-columns of a single pixel and all the p-columns of the sensor) is dominant and significantly increases as the number of columns is increased, resulting in higher noise.
- On the other hand, a larger number of columns corresponds to lower distance between the columns, so that it is easier to counteract trapping effects and to improve the charge collection efficiency.
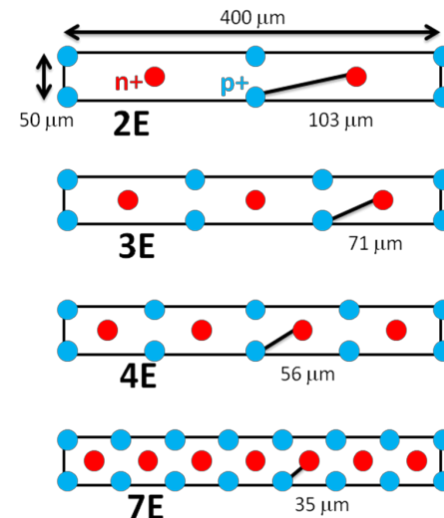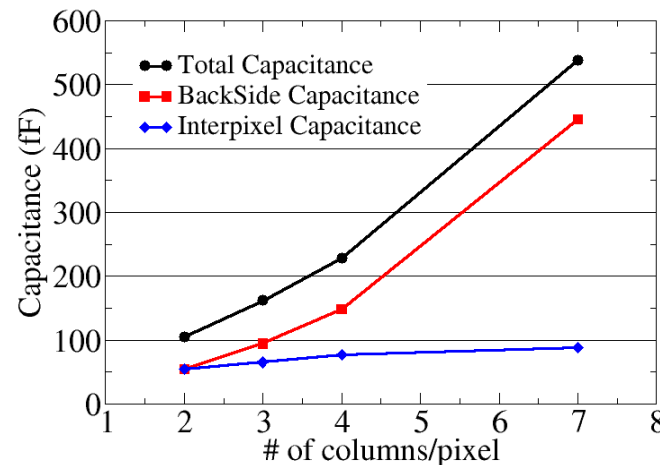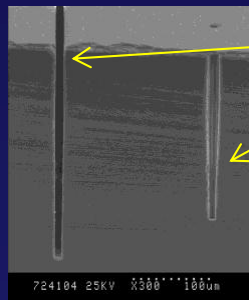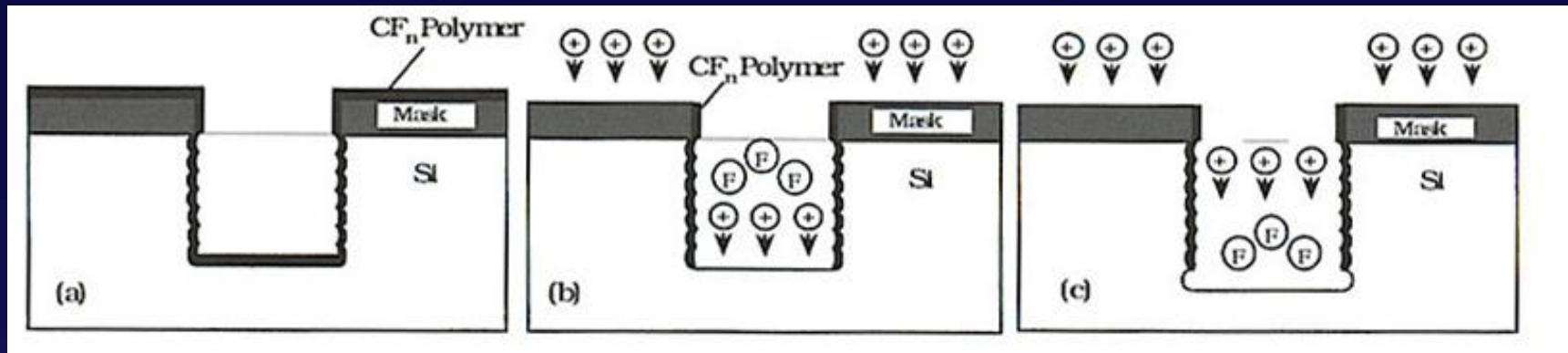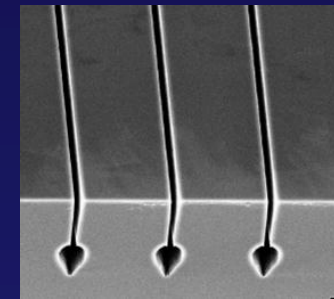

Fig.3 Simulated contributions to the total pixel capacitance of the backside and the interpixel capacitances for 4 types of proposed ATLAS FE-I3 pixels: 2E, 3E, 4E and 7E, having 2, 3, 4 and 7 junction (n) columns per pixel respectively.
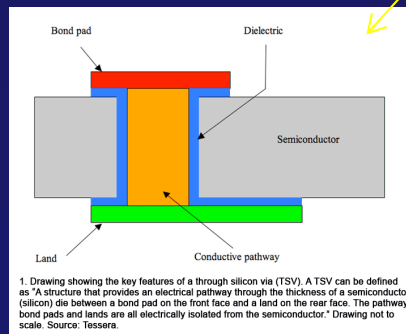
Microfabrication

For 3D sensors electrode definition and active edges
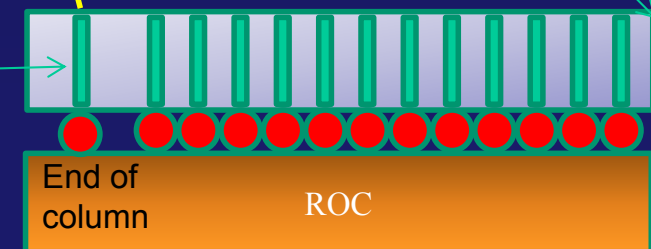
For cooling micro-channels

Interconnectivity Using TsV

Extra holes
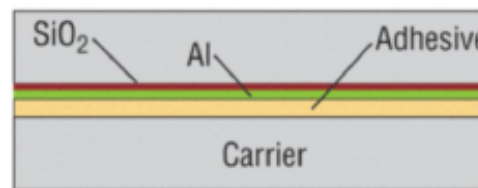On 3D sensor side
To carry signal out

1- conformal metal
2-doped poly (tests encouraging

End of column

ROC

1. Drawing showing the key features of a through silicon via (TSV). A TSV can be defined as "A structure that provides an electrical pathway through the thickness of a semiconductor (silicon) die between a bond pad on the front face and a land on the rear face. The pathway, bond pads and lands are all electrically isolated from the semiconductor." Drawing not to scale. Source: Tessera.

Bond pad   Dielectric

Semiconductor

Land   Conductive pathway

Cinzia Da Viá, Uni. Manchester, Trento Workshop 20th February 2013

Temporary bonding - brewer science® waferbond®

Bonding device wafer to a carrier to allow processing
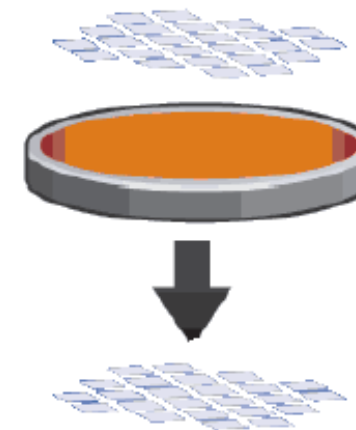
Through substrate patterning (eg. VIA)
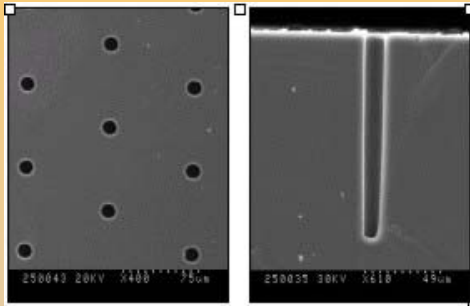
Patterning of through substrate structure

Release of carrier wafer

Similarly, sensors with active edges can have the support wafer removed when bonded to a carrier wafer, while sensors are release once the waferbond® is removed
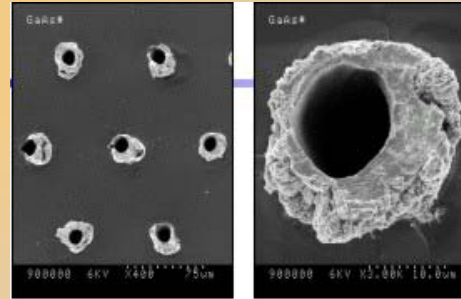
3D detectors: Excavating the holes
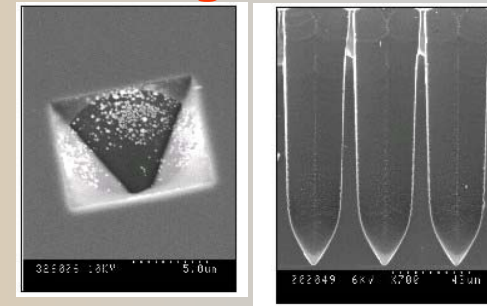
Dry Etching	Laser Drilling	Electrochemical etching
➢Standard photolithography process	➢ Any material ➢ No photolithography	➢No sidewall damage
➢Sidewall damage ➢Si and GaAs only	➢Slow process for big arrays ➢Sidewall damage ➢Tapering ➢Repeatability	➢Si only (GaAs and SiC?) ➢Complex photolithography
1μm / min.	1 hole / 3-5sec.	0.6μm / min.
Hole depth/diameter ~ 26	Hole depth/diameter: ~ 40 (but..)	Hole depth/diameter: ~ 25